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Open-source Design Tools for Sovereign Chip Development

Wolfgang Nebel, Robert Weigel (Eds.)

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Inhalt

Summary

Chip design is a key component in the development of innovative microelectronics and greater expertise in this field is vital to improving competitiveness and reducing Europe's and Germany's associated geopolitical vulnerability. To make the most of Germany's potential, the Federal Ministry of Research, Technology and Space **(BMFTR)**, is implementing targeted measures to strengthen the chip design ecosystem with the **Microelectronics Design Initiative.**

As part of the Microelectronics Design Initiative, the aim of the **DI-QDISC subproject** is to systematically analyse the potential and challenges of **open-source design tools for sovereign chip development** and to develop policy options for appropriate further development. This means investigating the ecosystem of open-source design resources and tools for electronic design automation (EDA) along the entire microelectronics development chain. The focus is on the current status of, development prospects for and existing obstacles to the use of these tools for analogue, RF, digital and mixed-signal design as well as for microelectromechanical systems (MEMS). In addition to technological aspects, attention is also being paid to economic and application-related issues.

Even today, open-source design tools are **complementing proprietary solutions** and contributing to European sovereignty in chip design, especially because of their central role in academic training and education. However, they are not yet capable of meeting every industrial requirement.

In both digital and analogue design, open-source design tools hold particular promise for **mature technology nodes** where open-source design tools can reduce barriers to entry by providing an easily accessible and inexpensive alternative to proprietary solutions for parts of the process chain, in particular at the design space exploration phase at the beginning of the design process.

Practical examples from education, research and industry have already demonstrated that **innovation mechanisms from the open-source software sector can be transferred to electronic design automation in microelectronics.** The innovation mechanisms used in open software development also have the potential in future to accelerate innovation processes in chip design. The largely intangible nature of chip design makes such an approach promising, as new solutions for design tools – similarly to AI research – can be transparently shared, tested and optimised.

Empowering small and medium-sized enterprises in chip design through open-source development tools is an important contribution to maintaining Germany's international competitive position in cutting-edge technologies. In comparison with other regions, Germany's technological performance has declined in recent years. Differentiating features in key industrial markets are increasingly being developed at the chip design level, which is why there is a need for deeper value creation through research and development.

The project group recommends the following measures to strengthen Germany's and Europe's **technological sovereignty and innovation capacity** in microelectronics and to establish a **self-supporting ecosystem for open-source design tools.**

- **Availability of skilled personnel:** in view of the impending loss of expertise due to retirement and the growing importance of microelectronics, training capacity at universities should be expanded in all areas relevant to chip design. Internationally competitive working conditions and programmes such as the Humboldt Professorships could attract top international talent to Germany. In addition, the next generation should have the opportunity to gain hands-on experience with open-source tools for chip design at an early stage as part of their own small chip development projects.
- **Industrial maturity by corporate participation:** an independent, largely industry-driven open-source EDA user forum (e.g. in the form of a foundation) could act as a central clearing house between users and developers in order to further develop open-source design tools in a targeted manner. Direct collaboration means common standards can be developed and seamlessly integrated into industrial processes. Embedded in a long-term semiconductor strategy, this could foster a market-driven innovation policy. In addition, when selecting chip design tools, companies should – where possible – give preference to those that support open standards to ensure compatibility with open-source solutions. It should always be checked whether internally developed solutions can be shared with the open-source community.
- **Government kick-start:** as part of its economic development initiatives, government could set up three programmes to support different points in the development ecosystem.

1. Government should support the establishment of a design platform as a "one-stop shop" to enable design, including for SMEs and start-ups. This platform should include an unbroken open-source tool chain and various offers for tape-outs. For companies wishing to make their own developments available

to the open-source community, **this "one-stop shop"** could guarantee long-term maintenance **as a trustworthy platform.** This organisation could also orchestrate the integration of new solutions and the further development of existing tools and host them on its own platform.

2. So far, German industry has played only a very minor role in the further development of open-source tools for chip development. A sponsored **EDA development voucher** is therefore proposed as an incentive to engage with open-source design tools alongside a corporation's actual core business and to develop them further to industrial maturity. If they have a use case, companies will be able to apply for a voucher that they can use to award development contracts for the further development of open-source EDA tools which will then be available under an open-source licence.

3. Europe's entire semiconductor ecosystem would benefit from the establishment of an unbroken development chain. Government support should therefore be provided for the development **of open-source PDKs,** for example 22 nm[1] at GlobalFoundries and 130 nm at IHP.

1 | Semiconductor technology manufacturing processes are typically described by the smallest structure sizes that can be produced photolithographically in nanometres (nm).

Project

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1 Microelectronics as key to economic prosperity and sovereignty

Microelectronics is the cornerstone of advanced technologies and a driving force for innovation and growth. In the more recent past, various crises have made it clear just how lacking in independence Germany and Europe are when it comes to microelectronics, and how significant this situation is. While chip fabrication is a matter of major political interest, what is often disregarded is that many stakeholders in the semiconductor sector are focused on the precursor to production, **chip design,** where a **substantial proportion of value creation and innovation** takes place.

To ensure security of supply of chips in established sectors, to develop new industries and to contribute to European **defence capabilities,** Germany – working together with other EU states – must revive lost chip design capabilities, strengthen existing capabilities and strategically develop new capabilities.

When it comes to **design tools** for semiconductor development, concentration of supply in the hands of a small number of major players has created an **oligopoly** with development centres located for the most part in the USA. Their proprietary tool chain often constitutes a high barrier to entry for smaller and new players. Open-source design tools are a highly promising alternative or supplement to established proprietary offerings. The potential of open-source design tools lies in particular in innovative chip development using proven production methods, as well as in the development of future computer architectures and technologies.

1.1 Geopolitical threats: significance of chip design for technological sovereignty

Microelectronics is not just one of many key technologies, it is the basis for all industries of the future. Economies that occupy only a few key positions in this industry not only have poor prospects for growth but can also easily **fall prey to foreign geopolitical interests**[2,3].

The current geopolitical climate calls Germany's entire economic and security policy architecture into question. The **nationalism and protectionism** which characterise the USA's "America First" **technology policy** is a turning point for free trade, while Russia's war of aggression against Ukraine has had the same effect regarding **security policy.** Multiple factors could jeopardise semiconductor supply and cause major harm. These include:

- the **"chip war"** between the USA and China,
- the Trump administration's **"America First policy"**,
- Xi Jinping's **"One China policy"**,
- possible **trade wars** and the supply of development tools and natural resources,
- secret backdoor **chip tampering** for espionage and cyber attack purposes,
- **Russia's arms build-up** and intimidation of NATO states and
- destruction of global microelectronic hubs at risk from **natural disasters.**

Microelectronics is the **driving force for economic innovation and growth.** As the basis for numerous applications – from automation and communication to artificial intelligence and defence capabilities – it is a key factor in achieving high levels of technological performance and competitiveness. Remote deactivation without mutual agreement of warheads delivered to Ukraine shows how vulnerable Europe is and how technologically dependent it is on the USA.

2 | See Miller 2023.
3 | See McKinsey Global Institute 2024.

German industry's great dependency on foreign microelectronic systems also poses a **risk to Germany's economic model and future prosperity.** The emergence of AI robotics within industry and of highly complex driver assistance systems for semi-autonomous vehicles means non-European competitors with microelectronics expertise are increasingly pushing at the doors of German industry. Just as was previously the case with battery technologies for use in e-mobility, German companies risk losing a major proportion of their value creation to non-European chip manufacturers which provide the corresponding digital platform technologies[4,5]. However, these hardware/software platforms require leading-edge chips with ultra-fine structures, and open-source design tools are not yet suitable for providing these.

Not only economic but also security policy considerations explain why Germany needs a **comprehensive industrial strategy** that is commensurate with the critical significance of microelectronics to prosperity and security and the same time takes full account of the important role of chip design[6,7]. Past experience has shown that other states, even allies, do not always take decisions with the interests of Germany and Europe in mind (see "E.I.S. Project" box).

In terms of value creation, chip design is one of the most lucrative business sectors within the semiconductor value creation chain: **design activities constitute 65 per cent of all R&D activities** in the value chain and **53 per cent of value creation**[8].

However, when it comes to EDA software and fabless design companies (such as NVIDIA or Qualcomm), the sector is dominated by American oligopolies, which control over two thirds of the market in terms of global sales revenue[9,10].

In particular, just a few major non-European companies, which primarily focus on their major customers, dominate the most recent technologies. The European Commission's targeted response to the issue of one-sided dependencies in chip design and fabrication and the massive state subsidy initiatives in competing economic regions is the European Chips Act (see European Chips Act box).

Technological sovereignty requires Europe to develop its own microelectronics and to assume a key position in global value chains, as this is the only way to reduce critical dependencies (through the use of a "bargaining chip"), to meet the most stringent security requirements, and to enable Europe to forge its own innovation pathways in cutting-edge technologies.

1.2 Strengths and weaknesses of the microelectronics industry in Germany and Europe

The field of semiconductor technology is divided into **different technology domains,** each of which constitutes a subsegment of the field (see figure 1). Germany and Europe have primarily specialised in those branches for which domestic customers can be found. These customers include, in particular, the automotive sector, energy technology and mechanical engineering. Chips for information technologies critical to sovereignty, on the other hand, are not part of the core business of the European Union's semiconductor companies; the companies in the semiconductor sector with the highest sales revenue are located in the USA and Asia[11].

The experts interviewed consider German and European industries to be competitive in **niche markets** such as power semiconductors, sensors, mixed-signal systems, microcontrollers, MEMS (microelectromechanical systems) and RF chips. European companies have even won a large global market share in microcontrollers (54 per cent) and sensor systems (41 per cent) but according to ZVEI (German Electrical and Digital Industry Association) the current situation is at risk due to a lack of industrial policy[12].

4 | See acatech 2024a.
5 | See Handelsblatt 2025a.
6 | See acatech 2024a.
7 | See acatech 2024b.
8 | See Boston Consulting Group/SIA 2021.
9 | See World Trade Organization 2023.
10 | See Boston Consulting Group/SIA 2021.
11 | See Statista 2025.
12 | See ZVEI & PwC 2024.

The “E.I.S. (integrated circuit design)” Project, Germany’s response to the initial technological contest for chip design dominance

As long ago as the 1980s, the geopolitical significance of the semiconductor industry led to trade conflicts, as the USA feared losing its technological dominance in this field (in particular to Japan) and thus also a central foundation of its military strength. The Soviet armed forces were numerically superior to the American forces but the USA were able to compensate for this disadvantage by using “smarter” microelectronically controlled systems such as satellites, stealth aircraft and cruise missiles, which made their armed forces more combat-effective[13].

Although Europe was not at the centre of this trade conflict around microelectronics in the 1980s, Germany and other allied European states nevertheless found themselves caught in the crossfire and felt the impact of President Ronald Reagan’s more protectionist foreign economic policy. As a consequence electronic design automation (EDA) tools were no longer unrestrictedly available for academic research purposes.

In response to international developments, and in order to catch up with the USA and Japan, the federal government initiated the national E.I.S. (integrated circuit design) Project, with the aim of strengthening academic research and so also making Germany’s domestic industry competitive[14].

A number of contemporary witnesses from the “E.I.S. times” report that the period saw some astonishing events that ranged from flying in American professors, who replicated American EDA software code at German institutions of higher education, to academics bringing unofficial copies of magnetic tapes holding sensitive data from American research institutions home with them in their luggage.

The E.I.S. Project oversaw the development of new methods and tools for designing integrated circuits and promoted cooperation between institutions of higher education, research institutions and industry. It also contributed to the training of specialists and laid important foundations for today’s German semiconductor industry.

For industry-oriented training and research, German institutions of higher education had access both to the largely open-source E.I.S. Tool Box (which in some cases also included proprietary/commercial programs) and to the ”VENUS” programme, a proprietary design system provided by Siemens (not the same entity as the current US subsidiary Siemens EDA)[15].

In addition to the national academic activities undertaken by the E.I.S. Project, industrial cooperation initiatives also came into being at European level, and can be seen as a precursor of the European Chips Act. The European Commission initiated a programme dubbed ESPRIT (European Strategic Programme for Research and Development in Information Technology)[16] with the aim of fostering information technology.

Germany took on a key role in Europe in the field of microelectronics, being the main coordinator in the development of design automation software and of a 1 megabit chip[17,18]. As part of ESPRIT, the companies Siemens, Bull and ICL additionally established a joint industrial research and development centre in Munich for mainframe computer architecture[19,20].

13 | See Shivakumar et al. 2022.
14 | See Abel et al. 1986.
15 | See ibid.
16 | See Cobby 2023.
17 | See Der Spiegel 1984.
18 | See Techmonitor 1989.
19 | See European Commission 1985.
20 | See Computerwoche 1988.

European Chips Act: enhancing technological performance, boosting resilience

The **European Chips Act** aims to enhance Europe's technological performance and boost supply chain resilience in the semiconductor sector. The Chips Act is based on **three pillars**[21]:

- **Chips for Europe Initiative:** support for research, development and innovation for advanced semiconductor and quantum technologies in the EU
- **Security of supply:** creation of a framework to strengthen production capacity, promote investment and secure semiconductor supply chains
- **European Semiconductor Board:** coordination between the EU Commission and Member States for monitoring the value chain and prevent and manage crises

The **first pillar** is critical to **supporting chip design** in Europe. The European Commission is planning to build a **cloud-based design platform** which will be accessible across Europe and will incorporate various design resources such as IP libraries and EDA tools. **Pilot lines** will also be created to enable the development, testing and small-batch production of new semiconductor technologies.

Media interest, however, is focused on the **second pillar,** in particular on **encouraging major foreign foundries to build fabs in Europe.** These are intended to strengthen Europe's security of supply in the event of geopolitical tensions.

While the USA and China and Far-East Asian economies such as Taiwan or South Korea have already been investing massively in their semiconductor industry and in building up capabilities in cutting-edge technology for decades[22], Germany and Europe have long done without any comparable **strategic national industrial policy** for maintaining or even deliberately expanding expertise. The European Chips Act has brought some change in this respect (see European Chips Act box).

The distortion of competition arising due to state interventions in other economies has resulted in the closure of **development divisions and production capacity** for leading-edge chips in Germany or in their being **taken over by non-European companies.** Since Qimonda went bust in 2009, Europe no longer has a DRAM manufacturer, and, following the demise of Siemens Mobile, Infineon's expertise in mobile radio chip design has been taken over first by Intel and then by Apple[23,24]. The German government's current coalition agreement sets out the intention to strengthen the country's microelectronics industry, placing specific emphasis on chip design.

In terms of export volumes, **Germany** has what is by far **Europe's largest microelectronics industry**[25] but, with the entire continent of Europe earning around 8 per cent of global microelectronics revenue according to data from 2020, the continent is in a relatively weak position compared with the USA (46 per cent) and South Korea (19 per cent)[26].

Despite their focus on niche markets, **Germany and Europe control only very few chokepoints**[27] in the global value chain and this applies both to chip design and to front-end/back-end fabrication. The capabilities and expertise available in the EU are

21 | See European Commission 2025.
22 | See Miller 2023.
23 | See WirtschaftsWoche 2024.
24 | See FAZ 2019.
25 | See Statista 2023.
26 | See Boston Consulting Group 2022.
27 | The term "chokepoint firms" is commonly used in the English-speaking world to denote companies that dominate essential technologies and are able to control access to specific products, services or technologies. They are able to create a monopoly or oligopoly, own crucial patents and establish high barriers to market entry, while other market players or entire sectors are heavily dependent on them.

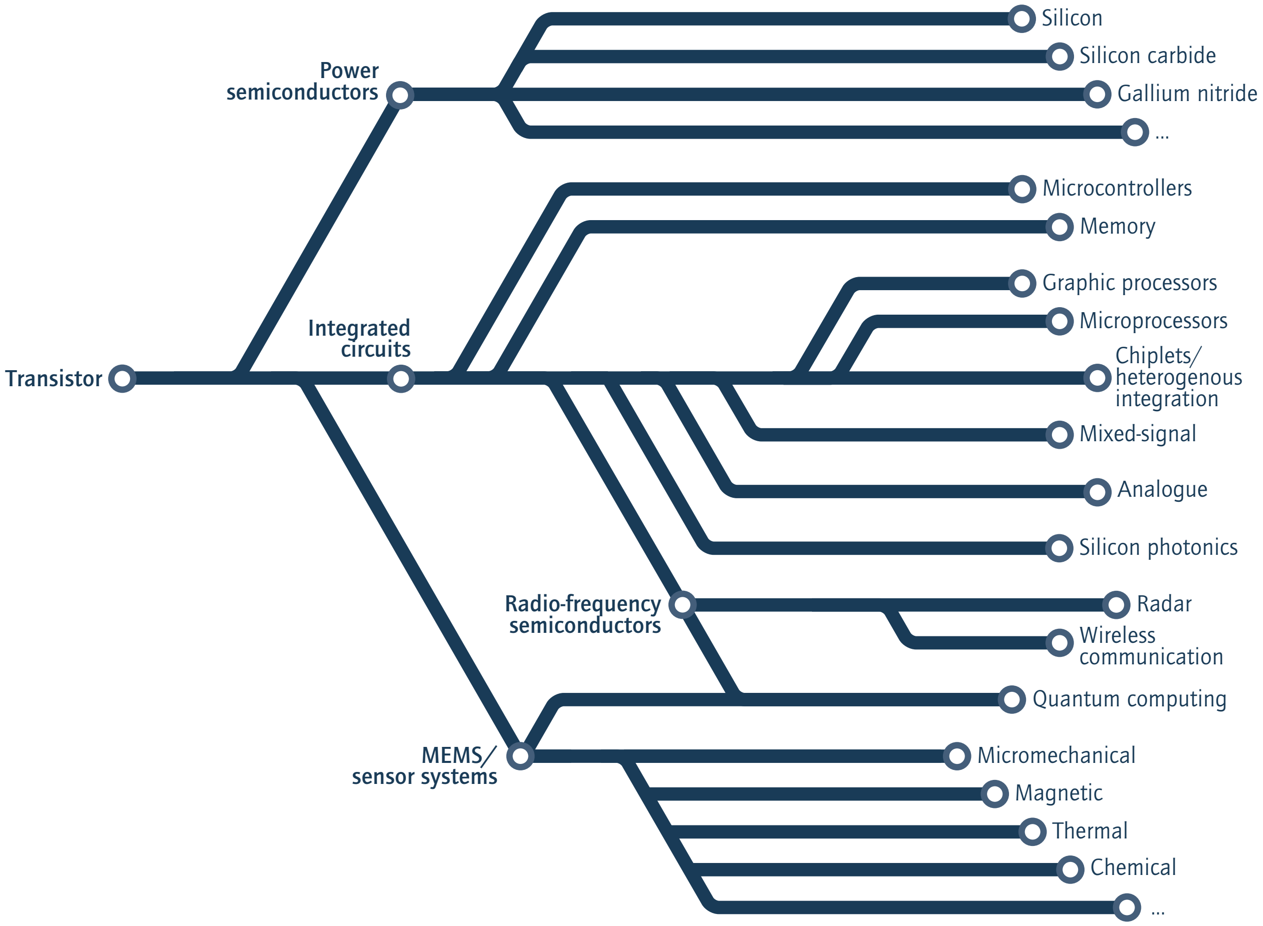

Figure 1: Semiconductor technology domains (source: own presentation based on Schumacher 2024)

also available in other economic areas[28,29,30]. Although Germany does have a large number of small and medium-sized enterprises which have established themselves in a narrow application niche and hold leading positions, constant global price and innovation pressure is increasingly eroding their position – especially with major European customers in the industrial automation and automotive sectors falling by the wayside.

The **German and European semiconductor industry's** relatively weak starting position is also linked to the **lower complexity product groups** in which the EU's semiconductor industry is heavily represented. The research and development expenditure of the three largest European semiconductor companies (Infineon, STMicroelectronics and NXP) combined is lower than the research and development budgets of individual US semiconductor firms[31,32]. Many small specialist chips – a traditional strength of European industry – are increasingly being replaced as technological development is being driven by fewer, but more complex, leading-edge chips.

It is precisely for these product groups with lesser complexity that very strong **competition is to be expected from China,** since China already today has the capability to manufacture such products largely autonomously[33]. According to analyses supplied by the Korea Institute for International Economic Policy (KIEP), China could, for example, have become the global leader in power semiconductors with innovative gallium nitride chips by 2033[34].

28 | See ZVEI & PwC 2024.
29 | See Germann et al. 2024.
30 | See World Trade Organization 2023.
31 | See European Commission 2024.
32 | See ibid.
33 | See Stroh 2025.
34 | See ElektronikPraxis 2023.

Mutual dependencies, on the other hand, can increase supply chain security. Although the global microelectronics ecosystem does include **some firms with German owners** that occupy a key position in the global semiconductor value creation chain and on which other states are at least to some extent dependent, these firms tend to be active in equipment and materials production and in EDA software and many of them are in fact USA-based subsidiaries **without significant business activity in Germany.**[35]

1.3 Open-source approaches as building blocks for innovative chip design ecosystems

Open-source tools for the design of digital circuits are a highly promising starting point for strengthening Germany's and Europe's microelectronics capabilities and reducing their one-sided dependencies. Proprietary solutions require compliance with **user and non-disclosure agreements,** which may limit latitude for action. In addition, how exactly they work is hidden behind the user interface, creating a vendor-lock-in situation and making optimum use of the tools more difficult. It is also difficult for SMEs and start-ups in particular to adapt these tools to their own requirements.

Open-source tools, on the other hand, allow **free use and adaptation** of the tools to user requirements and represent a highly promising approach to reducing existing obstacles in the field of software-based design tools and to helping to **build capacity** in this part of the value chain.

Proponents of **open-source design tools** point out the widespread acceptance of open-source approaches in the software field – in particular for data centres and telecommunications infrastructure – and see comparable potential for chip development. The experts interviewed consider this approach to have the following **positive characteristics:**

- **transparency and trust:** open-source code makes it possible to understand the reasoning behind design decisions, and allows the community to spot vulnerabilities or backdoors at an early stage
- **exchange of ideas and collaboration:** working together on solutions fosters collaboration between individual stakeholders
- **support for innovation:** open access allows researchers and developers to experiment more, build innovative approaches on existing solutions and so enables quick innovation cycles
- **competition:** open-source approaches can contribute to reducing the dominance of individual proprietary providers, with the provision of alternatives stimulating competition and preventing market monopolies
- **education:** open-source tools offer a favourable point of entry into chip design for universities and institutes of applied sciences, and open-source code may also contribute to a better understanding of technology
- **reputation and visibility:** open-source code can increase the renown of code developers, especially in the case of researchers at universities and other research institutions
- **reduced costs:** open-source tools and designs lower barriers to entry for companies and start-ups, since the cost of licences for proprietary tools can at least be reduced
- **flexibility and independence:** open-source tools can be adapted to a company's or developer's particular needs and requirements, with SMEs and start-ups in particular being less vulnerable to the power of oligopolistic market structures
- **interoperability and standardisation:** open-source projects can serve as the basis for open standards which improve interoperability between different tools, IP and fabrication processes.

However, the experts interviewed do also see **threats and challenges** resulting from the use of **open-source approaches:**

- **difficulties of integration and interface problems:** open-source tool mostly only cover individual steps in the design toolchain, meaning that tools have to be individually combined to provide coverage for the entire design toolchain, and so opening up the possibility of interface problems arising between the different stages of development
- **inadequate industrial maturity and limited functionality:** in addition to the problems of integration into existing design toolchains and development processes, some critical voices also bemoan the so far limited performance and speed of open-source tools
- **low level of acceptance:** since open-source tools have seldom previously been used in a commercial context, reservations about the quality and reliability of circuits produced using open-source tools are common
- **unclear legal situation:** while proprietary vendors enjoy a degree of user trust due to their many years of experience, open-source tools arouse concerns about liability, compliance and protection of IP, with customers and partners sometimes demanding the use of proven, certified tools
- **high financial risk:** high production costs in chip fabrication and very limited production capacities mean that faulty designs present an immense financial risk, which is a key

35 | See Germann et al. 2024.

difference in comparison to software, where faulty products can be patched, even after market launch; moreover, since there is as yet typically no evidence that open-source tools can produce functional designs in specific technologies, companies tend to shy away from being the first to bear the associated risk

- **inadequate leading-edge nodes:** there is a shortage of open-source design tools which are optimised for the requirements of ultra-modern fabrication processes, open-source solutions mostly only being offered for more mature technology nodes ranging from 130 nanometres (and larger) down to at most 45 nanometres
- **lack of PDKs:** elemental process data in the form of PDKs (process design kits) are tailored to the established proprietary tools and are generally only made available under an NDA (non-disclosure agreement), while open-source PDKs are only available for More than Moore technologies
- **limited support and development uncertainty:** while professional support is offered for proprietary tools, corresponding structures are not yet available for open-source solutions, meaning that personnel resources have to be allowed for on the maintenance and further development front
- **geopolitical conflicts:** some critical voices consider the worldwide availability of open-source design tools to be an economic and security risk due to the possibility of such resources being used by other stakeholders and nations, in particular the People's Republic of China.

Open-source approaches are considered to have particular potential in **new** semiconductor **technology domains.** The last few decades have seen innovation and value creation focus very strongly on the microprocessor sector and on miniaturisation (in terms of ever smaller structure widths) ("More Moore"), but this trend is increasingly coming up against physical limits.

In combination with the constant growth in energy consumption by large data centres, integration of different semiconductor components for **functional diversification** ("More than Moore") and **alternative computing technologies** such as analogue computing, optical computing or quantum computing are therefore becoming attractive ("Beyond Moore"). Against this background, Europe's heterogeneous technology landscape can be considered an advantage, but the necessary business and regulatory environment needs to be put in place and appropriate private and public capital provided if innovative research in the field of microelectronics is to be enabled. Open-source approaches could be ideally suited to this objective.

The **possible uses for open-source solutions** in various fields of application will be analysed below and their potential in sovereign chip development terms will be identified, paying attention to economically and legally viable business models.

Moore's law states that the number of transistors on a microchip doubles approximately every two years, with the result being exponential increases in performance and cost reductions per transistor. This principle has shaped the semiconductor industry for decades[36].

"More Moore" denotes conventional scaling according to Moore's Law, i.e. transistor miniaturisation and increased packing density on chips. This is based on developments in lithography (e.g. EUV technology) and new materials.

However, since purely scalar miniaturisation is now approaching its physical and economic limits, **"More than Moore"** approaches are becoming increasingly important. These focus on functional diversification such as chip stacking (3D integration), combining various technologies such as sensors, RF modules or memories on one chip (heterogeneous integration) and specialised processors (AI accelerators, edge computing chips).

"Beyond Moore" goes even further with research into new paradigms beyond conventional CMOS scaling[37], including, for example, quantum computing, silicon photonics or neuromorphic chips.

36 | See Moore 2020.
37 | See Dudek/Wirth 2025.

2 Microelectronics technology domains and chain

While public and political discussions around microelectronics frequently focus on the latest technologies for high-performance processors, it is often forgotten that there are many other technology domains in microelectronics that are particularly relevant to user industries in Germany and Europe. The various technology domains are therefore described below, followed by a general description of the design process for the two major classes. Section 3 then discusses open-source design tools against this background.

2.1 Microelectronics technology domains

The term **technology domains** describes the semiconductor technologies and corresponding integrated circuits (ICs) that are required for specific applications. The requirements placed on semiconductors in terms of electrical properties, geometric sizes, reliability etc. differ depending on the technology domain and the underlying semiconductor technology. The individual technology domains shown in figure 1 are explained below, together with their respective characteristics and special features.

Digital (microprocessors, graphics processors, microcontrollers and other digital ICs, FPGAs): digital circuits dominate almost all microelectronic systems and are the most widely used type of circuit. In contrast with analogue circuits, which process continuous signals, digital circuits operate with discrete values that are typically represented by the binary states 0 and 1. This mode of operation offers a high signal-to-noise ratio together with easy and reliable data storage. Digital circuits are distinguished by robustness and scalability, allowing them to exploit to the full the potential of the latest leading-edge technologies in the nanometre range. Their binary data processing makes them less sensitive to noise and to component tolerances. The advanced level of electronic design automation (EDA) for digital circuits is a significant advantage. This automation is built on solid mathematical foundations (Boolean algebra) together with advanced models and algorithms, and thus enables efficient development and optimisation of digital systems. Electronic design automation covers all design phases, from system design through logic design to physical design, including placement and routing. Besides processors, many simpler functions such as digital filters, counters, automatic devices for control systems, arithmetic and logical functions etc. are replicated by digital circuits.

Field-programmable gate arrays (FPGAs) are a specific class of integrated circuit and are mainly used in **digital circuit implementation.** FPGAs offer greater flexibility than conventional application-specific integrated circuits (ASICs) as their functionality can be reconfigured and adapted without additional fabrication steps. To a degree, therefore, they are similar to software-programmed processors. FPGAs consist of numerous programmable logic blocks connected together by a configurable network. These logic blocks can be programmed to carry out different logical functions. Highly complex digital circuits can be created by appropriately interconnecting the blocks. The main advantages of FPGAs include their great flexibility, which allows them to be straightforwardly adapted to new requirements, a simplified design process (design stages such as timing analysis are simplified or dispensed with (sign-off and mask production)), and short development times. They also benefit from comparatively low costs as there is no need for complex chip fabrication in the event of changes in functionality. Nonetheless, they do also have some drawbacks compared to ASICs, these including lower clock frequency, larger area and higher energy consumption. When produced in very large numbers, FPGAs are also more expensive than ASIC solutions. FPGAs are used in a wide range of applications, for example in prototype development, as well as for relatively small production runs (under ~ 100,000 chips, depending on the technology) and where there is a need for subsequent modification (e.g. adaptation to protocols), in fields such as telecommunications and network engineering, aerospace, satellite technology, data centres and medical technology.

Analogue: unlike digital circuits, analogue circuits process continuous signals and are used in many applications. Examples of analogue circuits are (signal) amplifiers (for instance operational amplifiers), (signal) filters (e.g. low pass, high pass and bandpass filters), oscillators, voltage regulators, analogue-to-digital converters (ADCs), digital-to-analogue converters (DACs) and modulators and demodulators. Analogue circuits can be put to use in a vast number of areas, for example in sensor systems, audio, communications and medical technology, metrology, and open- and closed-loop control systems. Compared with digital circuits, which offer a high signal-to-noise ratio, analogue circuits are more susceptible to noise, non-linearities, temperature dependencies, parameter drift, component tolerances and parasitic effects. These characteristics significantly complicate the design and optimisation of analogue circuits. In addition, electronic design automation is markedly more limited with analogue circuits than with digital circuits. Automated design tools are predominantly available for smaller units such as operational amplifiers. Moreover, analogue circuits do not benefit from leading-edge technologies to the same degree as digital circuits as their performance is often more heavily dependent on physical effects and component parameters than on technology scaling.

RF: RF (radio-frequency) circuits are a particular type of analogue circuit designed for operation in the high-frequency range and play a central role in communications technology. Typical RF circuits include radio-frequency amplifiers, mixers, filters and oscillators. Since physical effects occur at high frequencies which are negligible at lower frequencies, the design of RF circuits differs in many aspects from that of analogue circuits which are designed for these lower frequencies. High-frequency effects which need careful consideration when using RF circuits include the parasitic characteristics of capacitors and inductors as well as electromagnetic interactions. RF circuit development therefore requires an in-depth understanding of the complexities of high-frequency technology.

Mixed-signal: mixed-signal circuits are a combination of digital and analogue circuits. Examples of such circuits are analogue-to-digital converters (ADCs) and digital-to-analogue converters (DACs). Strictly speaking, almost all of today's semiconductor chips are mixed-signal circuits, since even digital circuits need analogue components such as oscillators, for example for clock generation.

Memories: memories are mixed-signal circuits since they contain both analogue (e.g. sense amplifiers) and digital components (e.g. decoders). There are many different types of memory, the fundamental distinction being between volatile storage devices (e.g. static random-access memory, or SRAM for short, and dynamic random-access memory, DRAM for short), which lose the stored values when the supply voltage is turned off, and non-volatile memories (for instance flash memories), which provide permanent data storage.

In contrast with digital technologies, which are primarily optimised for speed, the main purpose with memories is to maximise storage density and minimise cost per stored bit. The fabrication technologies for memories, such as flash and DRAM, accordingly differ from those used for digital circuits. Use may additionally be made of special elements such as floating-gate transistors or resistive random-access memory (RRAM). These elements are crucial for data storage and have a major influence on the characteristics of the respective storage technology. Memory design has many parallels with the design of analogue circuits, as it requires accurate management of analogue signals and effects.

Power electronics: technically, power electronics belongs to the category of analogue circuits, but differs in its focus on switching and control of high electrical currents and voltages. It uses special power semiconductors such as power diodes, insulated-gate bipolar transistors (IGBTs) and thyristors, which were developed specifically for these purposes. Besides conventional silicon technology, new semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) are increasingly being used. These materials offer decisive advantages, including higher efficiency, better thermal properties and greater electric strength, making them particularly suitable for demanding applications. Power electronics is used in numerous fields of application, for instance electromobility, renewable energies and in industrial applications such as motor control and energy conversion systems. However, power semiconductors are significantly larger in size, with a markedly lower integration density. This is due to the physical requirements associated with processing high powers, and to the need for effective management of the waste heat caused by the high power. 3D simulations, which require nonlinear differential equations to be solved, are a central tool in the development of power electronics circuits. Power electronics circuit development demands an in-depth understanding of the semiconductor technology used.

Silicon photonics: while in conventional circuitry, electrons form the basis for electrical signal transmission and processing, photonic systems are based on light, or photons. Silicon photonics integrates optical components into proven silicon technology. By using light for data transmission and processing, systems can potentially achieve higher speeds and a consume less energy. With silicon photonics, optical waveguides, modulators and detectors are developed directly on silicon chips, to enable a seamless connection between electronic and optical functions. When used in sensor systems they allow high-precision measurements, for instance for temperature, pressure or chemical composition detection because a change in the variable being measured modifies the optical behaviour of the measuring system. Furthermore, photonic technologies play a central role in quantum computing, where photons can be used to transmit and manipulate quantum information. Approaches based on photonics are also increasingly being used in analogue computing. However, the development of photonic systems is a technical challenge, since it requires the integration of optical and electronic components. Design tools for photonics are therefore very specific and also have only a relatively narrow range of users.

MEMS and sensor systems: MEMS circuits are not circuits in the conventional sense, rather they are microelectromechanical systems (MEMS) which combine electronic circuits and mechanical structures on a single chip. MEMS systems use various physical effects – mechanical, electrical, thermal or fluid-dynamic – to generate electrical signals which then undergo further analogue and/or digital processing. Typical examples of MEMS are acceleration or pressure sensors, which are used in automotive technology, medical technology and process automation. They are also used in microfluidic systems that are put to use, for example, for chemical analyses or in medical technology. Due to the multiphysical nature of MEMS systems, their design is highly dependent on the particular physical effect being utilised. This requires the use of complex simulation methods. In addition, the integration of MEMS structures and electronic circuits on one chip is a particular technical challenge.

Chiplets/heterogeneous integration: chiplets are a comparatively new form of implementation – instead of using a single large monolithic chip, a number of smaller chips, or chiplets, with different functions and sometimes from different technology domains are combined on a common substrate or in a package. This method offers numerous advantages. For instance, the smaller sizes of the individual chiplets result in a higher yield while the ability to use the most ideally suitable technology for each chiplet improves cost-efficiency. Chiplets also enable heterogeneous integration, i.e. integration in one component of elements produced using different technologies. The limits to maximum chip size resulting from exposure technology can also be overcome, with chiplet designs also benefiting from better scalability and flexibility. However, despite these advantages, the implementation and integration of chiplets is not without its challenges, the most serious being ensuring high-quality connections between the chiplets, the low overhead for die-to-die interconnects, thermal management, testing, increased design complexity and interface standardisation. Since this approach is comparatively new, only a few suitable design tools are available for efficient development of this technology.

2.2 The microelectronics technology chain

Before open-source tools for chip design are discussed in detail in section 3, this subsection will describe the steps needed to develop a semiconductor chip. A significant aspect in this regard is that the semiconductor production plants (**"fabs"**[38]) so frequently discussed by policy makers and the public are just one element of the microelectronics value chain – actual semiconductor fabrication is preceded by chip design. Current chip designs sometimes consist of over 100 billion interconnected transistors, meaning that they can only be developed using special computer programs known as electronic design automation (EDA) tools. This means a major part of semiconductor development plays out in virtual space, not unlike conventional software development.

Once chips have been fabricated in fabs they have to be **packaged & tested,** i.e. the unprotected semiconductor chips (or "dies") are encapsulated in packages and tested to ensure functionality. Advanced packaging enables the integration of different semiconductor technologies on a single substrate. Heterogeneous integration can combine specialised chips – for instance high-power logic, memories, analogue components or AI accelerators – in a single solution, so improving energy efficiency and performance and reducing latency by moving components closer together. Advanced packaging and heterogeneous integration of the final product need to be considered right from the design phase. Figure 2 shows the individual steps in the semiconductor chip development process.

IP: rather than starting from scratch, the development of new designs – like software development – frequently involves the use of existing and tested elements, for example processor cores, signal processing units or complete subsystems. These prefabricated elements constitute "intellectual property (IP)".

38 | "Fab" is an abbreviation for (semiconductor) "fabrication facility".

Libraries: libraries contain fundamental, often standardised building blocks such as logic gates (standard cells), I/O cells, memory cells and basic analogue structures. While IP elements are mostly independent of the fabrication process, libraries define how the abstract standard building blocks are implemented in the respective specific fabrication process, and thus constitute a central basis of the design process.

PDK: since chip design must essentially comply with the possibilities offered by the fabrication partners in the respective fab (e.g. with regard to possible structure width), these constraints have to be considered right from the design stage. The collection of relevant information is known as a process design kit (PDK). These datasets are often jealously guarded by the fabs and only shared once legal protections are in place as they allow conclusions to be drawn about a fab's capabilities in the highly competitive field of semiconductor fabrication.

ADK: while interest previously mainly focused on the fabrication parameters contained in the PDKs for the chips themselves, the focus has more recently shifted to more complex packaging strategies, for example using chiplets, which allow greater integration density and the combination of different technology domains. Information relevant to these steps is compiled in assembly design kits (ADKs).

2.2.1 Electronic design automation for digital circuits

In recent decades, electronic design automation of digital circuits has become the dominant technology domain in chip design, as the microprocessors developed using it are more flexible programmable and are very easily Moore's-law scalable. Although this development is slowly coming up against its physical limits and alternative technologies are being considered, digital design continues to be the most important technology domain. Figure 3 shows the design toolchain for digital circuit design while the individual elements from the figure will be described below.

Architecture and system design: electronic system level design starts with specification of the applications to be implemented and of a (system) architecture for implementing these

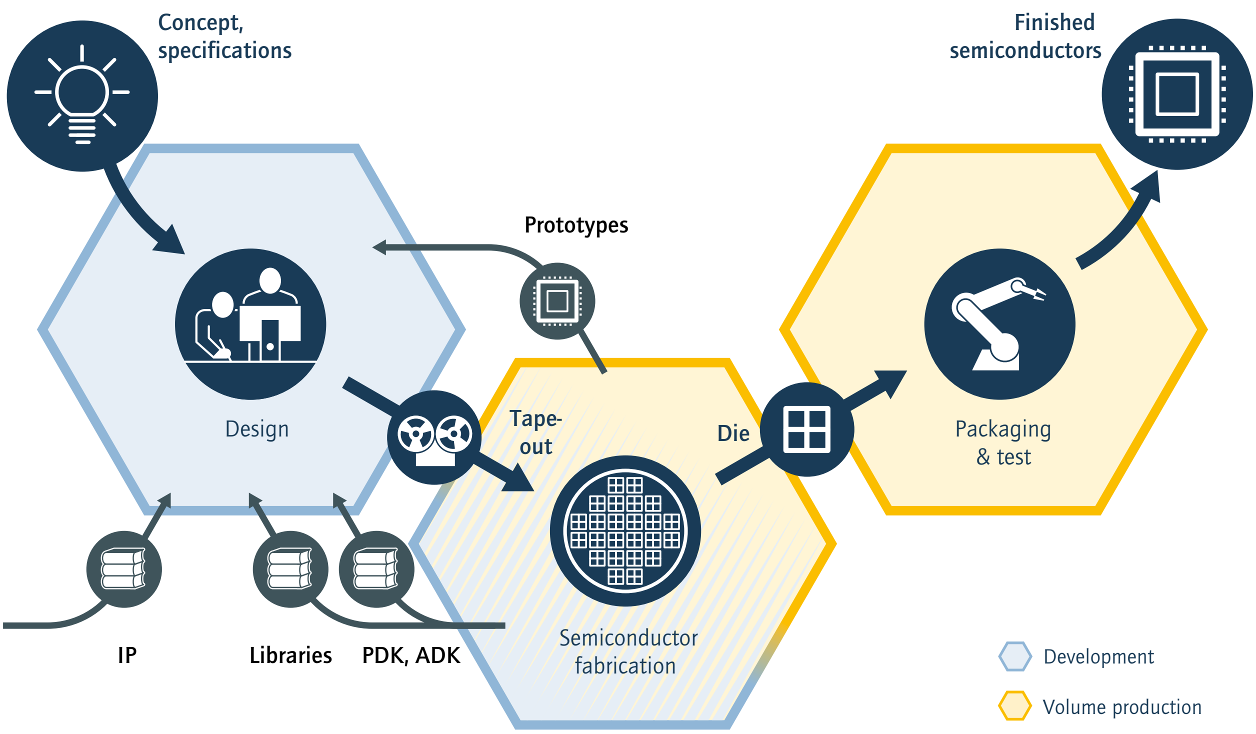

Figure 2: Design steps in semiconductor chip development (source: own presentation)

applications. Examples of the questions to be addressed are the maximum number of which processors the chip is to have, which memory types and sizes are to be instantiated and what peripherals (interfaces to the outside) the chip should have.

Nowadays, modern "hardware/software co-design"[39] tools make a significant contribution to automating system synthesis: this involves exploring design alternatives, optimising system configuration (e.g. analogue versus digital, software versus hardware) and optimised mapping of the applications onto the system architecture taking account of important design limitations such as chip cost, performance boundaries to be adhered to, etc.

Synthesis: synthesis involves translating the abstract design into a technology-dependent gate-level netlist. This contains instances of prefabricated circuit elements taken from libraries, and defines how these circuit elements are electrically interconnected. Physical limits and requirements, such as the electrical resistance of a specific interconnect, have to be taken into account.

Place and route: the provision of the gate-level netlist is not the end of the hardware design step. The individual elements of the gate-level netlist are arranged on a two-dimensional surface, which can be thought of as a virtual chip. Furthermore, contact pads have to be integrated to provide the chip with an interface to the outside world, as does a power supply for the elements and the routing of specific signals, for example the clock pulse. This task involves running highly complex algorithms on millions or even trillions of data elements, a process which is very demanding in terms of software implementation. To share out the enormous volume of data to be calculated, placement first involves drawing up a rough arrangement of elements, or "floor plan".

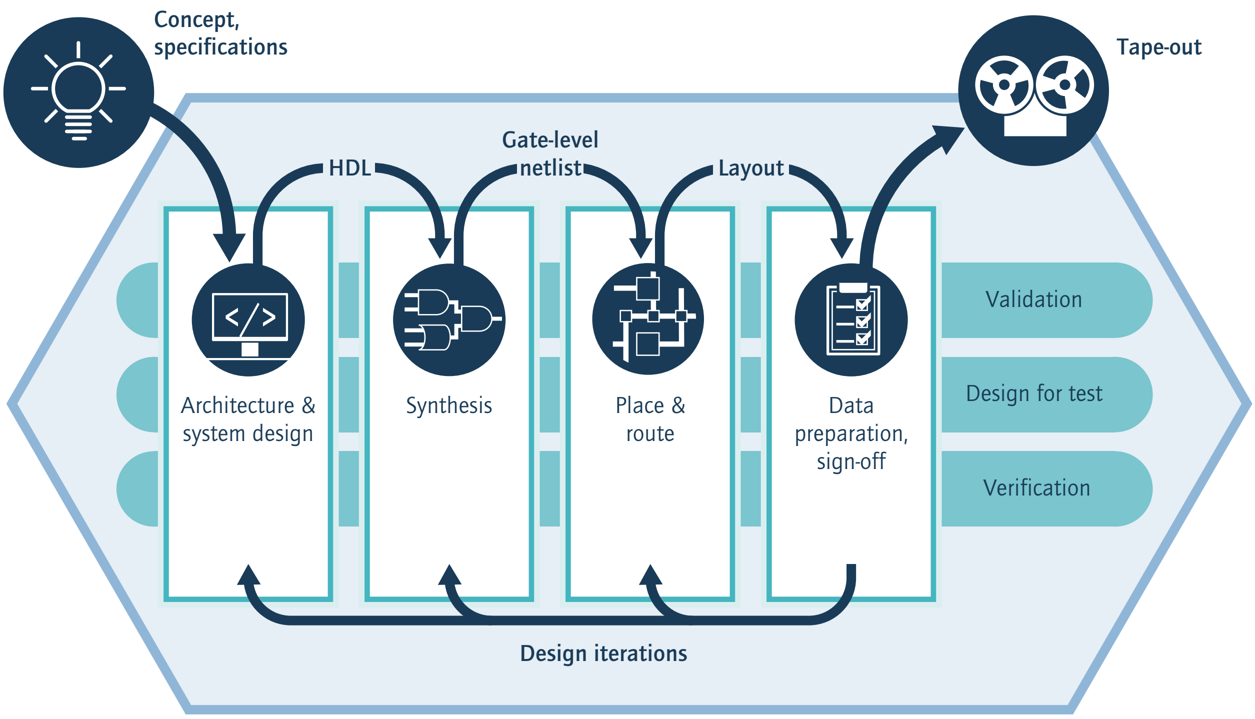

Figure 3: Design process for digital circuits (semicustom design flow; source: own presentation)

39 | See Teich 2012.

Data preparation, sign-off: once an ideal representation of structure and arrangement has been generated in the preceding steps, fabrication-specific checks are finally carried out as well as transformations for producing exposure masks for fabrication. Due to the small structures on the chips, the masks do not reproduce the desired structure on a one-to-one basis but rather are configured to achieve the targeted structure as closely as possible taking account of the knowledge of the fabrication processes.

Validation: this encompasses all the steps involved in ensuring that the design corresponds functionally to the requirements of use, will be stable over time and is physically fit for fabrication. These steps include functional verification (simulation and formal methods), logic equivalence checking (LEC), and a timing analysis (STA) for checking signal paths. Power analyses are also carried out to optimise power consumption. Placement and routing are followed by a physical verification (DRC/LVS) and finally a sign-off validation, after which the design is sent for fabrication.

Design for test: as semiconductors involve such very small structures, 100 per cent correct fabrication cannot be ensured, even with established technologies. Comprehensive tests are needed to detect fabrication errors and discard faulty chips, or to activate redundant structures inside chips. These are highly complex and account for a substantial proportion of fabrication costs[40].

Verification: verification describes the process of checking whether the design fulfils functional specifications. While validation ensures that the design meets the requirements of the final product, verification is focused on whether the design has been correctly implemented. The process involves simulations, formal verification and hardware emulation, in order to detect errors at an early stage. Verification takes place at various levels, from register transfer level (RTL) to gate-level simulation, and encompasses methods such as unit tests, system verification and coverage analyses, so as to ensure that all design cases are covered.

After final verification, the **masks and test data** are sent to the fab, a step known as tape-out on the basis of the magnetic tapes used in the past as data media.

2.2.2 Electronic design automation for analogue circuits

A further important technology domain in chip design is **analogue technology.** While digital circuits process information in discretised binary form (ones and zeros), for many applications it is more sensible to process continuous, infinitely variable information, and in such cases analogue circuits are used. The design toolchain for analogue circuits, illustrated in figure 4, will be described below.

Architecture, schematic/netlist entry: as with digital design, the design process for analogue circuits starts with an abstract description of the architecture, presented as a circuit diagram (schematic) or netlist. Although this format only allows the elements and their links to be specified, and not their spatial arrangement on the chip, it constitutes the essential basis for development of an analogue circuit. The circuit diagram is used to simulate the characteristics of the analogue circuit and so estimate the necessary dimensions of the components.

Custom layout design: the circuit diagram or netlist is used to create a custom layout which establishes the geometric arrangement of the elements on the chip. While in digital design this step can be carried out in a highly automated manner due to the robust discrete signals (ones or zeros) involved, in the case of continuous analogue signals, effects such as conduction losses and interference from adjacent elements have to be considered. This requires solid experience, which explains why this process is often performed manually for analogue circuits.

Physical verification, parasitic extraction: once the custom layout has been created, the necessary checking steps can be performed. Design rules have to be checked to ensure that the layout lies within the fab's fabrication tolerances. The layout also has to be compared with the circuit diagram to ensure compliance with the simulated dimensions and that all interconnects in the layout correspond to those in the circuit diagram.

Once the layout has been completed, interference effects, or "parasitics", are simulated in a dedicated step. If such interference restricts chip function, iterative loops can be used to adapt the circuit design or layout accordingly. This process is repeated until the parasitics are of a manageable order of magnitude and as soon as processes are complete, the design can be handed over to the fab in the form of masks and test data.

40 | See West 2020.

Simulation: while in digital design, signals are generally binary and the formal verification process detects many errors at an early stage, in analogue design, continuous-value simulations are indispensable. Analogue circuits process continuous signals and are greatly influenced by nonlinear components, parasitic effects and environmental factors such as temperature or noise. Since they cannot be all that readily abstracted or systematically tested, detailed SPICE simulations[41] are needed in order to predict behaviour such as amplification, distortion or tolerance deviations. Methods such as transient, frequency and Monte Carlo analyses assist in optimising the circuit under real-life operating conditions and in ensuring that it functions reliably.

The other parallel processes of **validation, design for test, final verification** and **sign-off** are comparable with digital design and have already been described above.

2.2.3 Packaging & test

After fabrication and singulation in the fab, the highly sensitive semiconductor elements have to be encapsulated in packages so as to protect them from mechanical and electrical influences. This does not usually take place in the fab itself but rather is taken care of by specialist companies. Like fabs, for cost reasons these are often located in Asia, making this fabrication step vulnerable to geopolitical crises.

While in the past individual **dies** were generally encapsulated in a package, more recently the **chiplet** concept has become increasingly popular, involving, as it does, obtaining high integration density by integrating multiple elements into a multichip system. Figure 5 shows both process flows.

Die test: before the individual dies are encased in a casing, they may undergo functional testing. This step is optional, and depends on the packaging costs of faulty dies as compared with the cost of a die test.

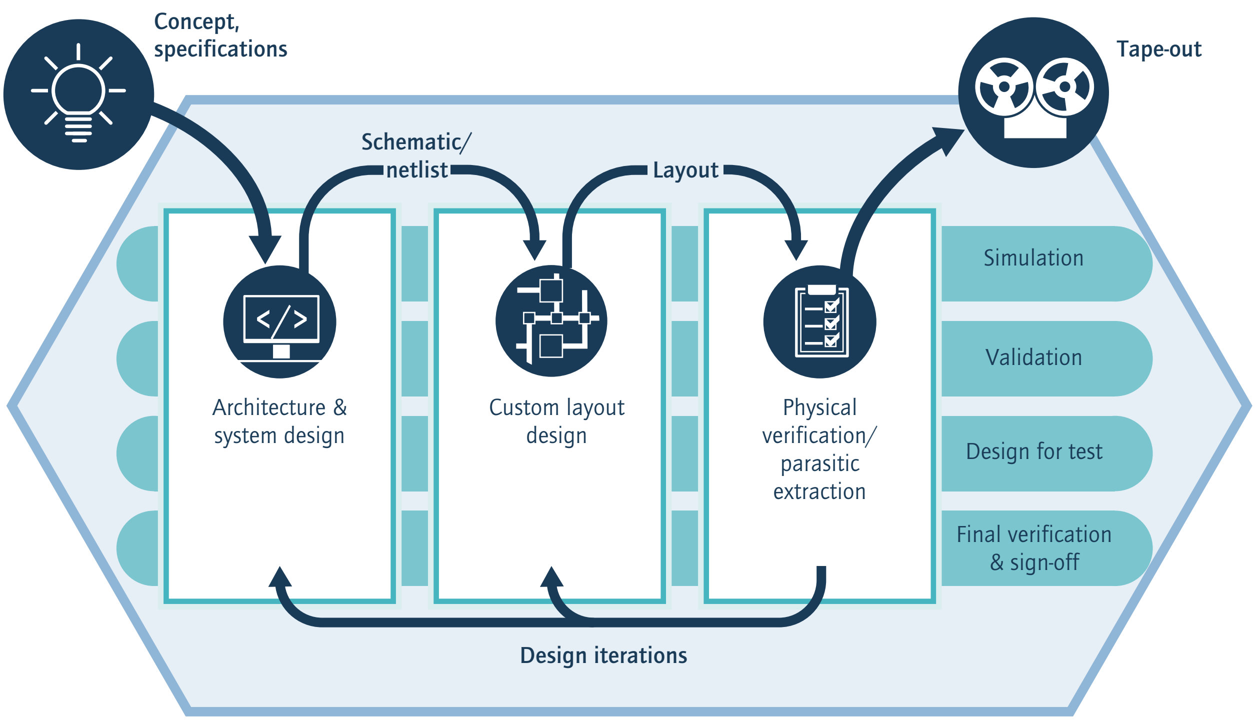

Figure 4: Design process for analogue circuits (custom design flow) (source: own presentation)

41 | The acronym "SPICE" stands for simulation program with integrated circuit emphasis, i.e. it is software for simulating electrical circuits.

Packaging: in this step, the contacts of the dies are contacted with fine wires or solder balls and encapsulated. The chip's semiconductor core is then protected from external influences.

Chiplet test: for some years now, the approach has increasingly been adopted of combining multiple elements – often from different technology domains (e.g. a laser element, an RF element and a logic element) – in a single package to produce an integrated multichip system. The individual elements are then known as chiplets. Since a faulty chiplet would compromise the entire system, chiplets are tested separately prior to integration.

2.5D/3D heterointegration: in this step, the individual chiplets are integrated with one another to produce a multichip system. Depending on the component, the elements may be arranged next to or above one another to enable optimum functionality.

Final test: the final step of both process flows is a final, definitive check with documentation of chip functionality. Once this is complete, the finished semiconductors are installed for their intended application and put to use.

Although the processes illustrated in figures 2 to 5 have been greatly simplified, they do give an impression of the **complexity** and **effort** involved in **chip design,** which is only possible with highly specialised computer programs and appropriately trained and experienced specialised personnel. Given the high costs, more and more companies have taken to purchasing the development tools, or even the finished chips, rather than working on costly in-house developments. The reduced opportunities for optimisation that this involves lead to compromises in terms of function, costs and market differentiation. It has also led – especially in the field of development tools – to concentration in the hands of just a few providers, whose oligopolistic position, while a nuisance for large European enterprises, is an insurmountable barrier for SMEs and start-ups. An alternative approach to these proprietary design tools will be presented in the next section.

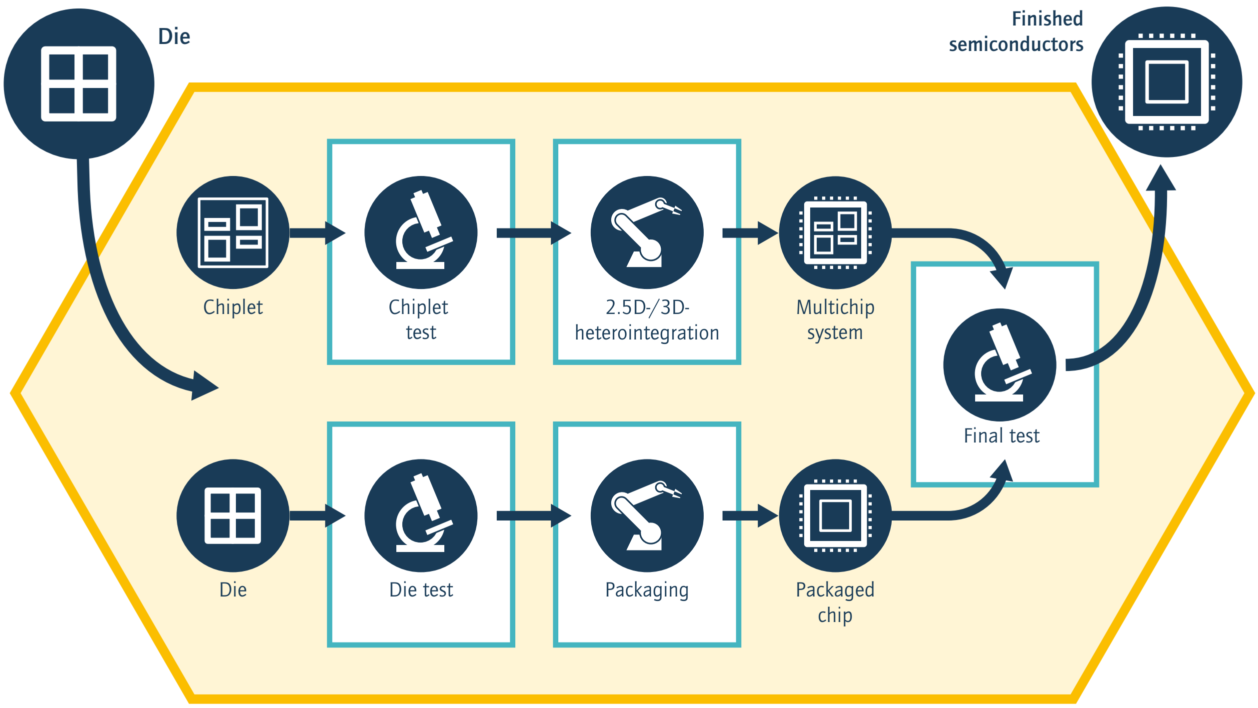

Figure 5: Process flow for packaging & test (source: own presentation)

3 Open-source approaches for design tools

Chip design is a largely **intangible development process** that to a great extent resembles software development practices more than practical development work with mechanical assemblies in the design process of physical devices and systems (see section 2).

Electronic design automation tools in microelectronics are software and therefore the **principles of open-source software development** can be transferred to some extent. However, it must be borne in mind that open-source EDA software is very much a niche area in comparison with general software and the developer community is significantly smaller.

While the licence costs of proprietary chip design tools are in no way negligible, saving on these costs is not the primary focus for many of the interviewed proponents of open-source design tools. Rather, they consider the development structures of open-source hardware IP and open-source development tools to offer an **innovation framework** that can break down the rigid structures involved in proprietary design tools with their strict terms of use and non-disclosure agreements and enable technological breakthroughs.

As long ago as the late 1960s, Melvin Conway made the observation that the **structures of development organisations** are reflected in the **characteristics of the products they design.** In a paper entitled "How Do Committees Invent?" Conway[42] states:

> "... organizations which design systems (in the broad sense used here) are constrained to produce designs which are copies of the communication structures of these organizations."

The debate around the influence of organisational structures on technological development is currently centred on the concept of **frictionless reproducibility.** David Donoho understands this to mean that scientific findings can be reproduced without impediment and that this can act as the foundation for continuous improvement. In relation to AI, frictionless reproducibility is built on three pillars, which are also reflected in the organisational structures of open-source. [43,44]

Data: data should be easily accessible and shareable.

Code: the code for processing the data should be easy to execute.

Competition: evaluation should be carried out by competitive testing.

The mechanism underlying frictionless reproducibility spurs on **scientific and technological progress** by enabling **numerous parallel experiments and optimisations.** Small modifications are tested and, if found to be improvements, act as the starting points for further research. This iterative, decentralised approach based on the publication and reproduction of findings makes it possible to work together in coopetition towards better solutions. A widely held theory is that it is the mechanisms of frictionless reproducibility that have made the current breakthroughs in artificial intelligence possible in the first place because the right conditions have only been in place since the internet has been in widespread use and sufficient computing capacity has become generally available.

The experts interviewed consider that frictionless reproducibility in chip design and the development of chip design tools is still in its **infancy.** However, it can plausibly be assumed that a similar revolution could also be possible in this field if chip designs (IP) and chip design methods (EDA tools) were freely shared and compared, as has happened with artificial intelligence methods.

Building on the technical explanations about the chip design process in section 2, **subsection 3.1** presents and briefly explains **available open-source chip design tools**.

Drawing on this report of the current situation, the most urgent action areas are firstly identified, after which a **vision** taking account of the *Open Source EDA Roadmap* for Europe is developed.

The success of open-source design tools is largely dependent on their widespread use and on business models capable of providing the considerable resources required for development and maintenance. **Subsection 3.2** examines the **value creation aspect and motivation** to use open-source design tools in relation to education and research, industrial applications and commercial providers of open-source solutions.

42 | See Conway 1968.
43 | See Donoho 2024.
44 | See Recht 2024.

Since the mechanisms of frictionless reproducibility are largely based on non-technical factors, the focus in **subsection 3.3** is on the **governance** of open-source ecosystems, specific legal requirements and the importance of standardisation processes. The section concludes with a presentation of the accompanying measures that government can put in place to support the development of a self-sustaining ecosystem in Germany and Europe.

3.1 Vision for an open-source tool chain

While open-source tools have been in existence for some time for individual steps in the design toolchain shown in figures 2 to 5, until a few years ago **it was not possible to progress along the entire process chain of semiconductor development using only open-source tools.** Using open-source tools always involved considerable additional effort in order to integrate them manually into the existing proprietary design toolchains, so constituting an obstacle in organisational and economic terms. This is why the effects of frictionless reproducibility have not yet become apparent in microelectronics.

In recent years, a completely open-source digital design toolchain has been developed – in particular through ETH Zurich activity as part of the "PULP Platform"[45] – and as a result the first successful examples of designs developed entirely with open-source tools are now available. However, the landscape of open-source design tools remains fragmented and incomplete for key technology domains. For this reason, the **vision of a complete open-source design toolchain down to the 22 nm node** is still being pursued. In addition to the EDA tools that are key to circuit design, a completely open-source design toolchain also requires attention to be given to "IP", "libraries" and "PDKs" or "ADKs".

Open-source IP is only available to a limited extent. Even circuits that have been common for years or decades often have to be recreated, purchased or licensed. One of the reasons for this is that IP frequently relates to a specific fabrication process, the PDK of which is covered by non-disclosure agreements that prohibit free publication of the IP. While established companies can draw on their own pool of already developed IP, new players must first develop or license the IP themselves.

Open-source libraries and PDKs are not common as the information they contain provides an insight into and allows conclusions to be drawn about the fab's technology. What's more, the conclusion of non-disclosure agreements (NDAs) is the rule, which constitutes a barrier to open-source design flows.[46]

Exceptions include open-source approaches such as the 130 nm SkyWater Open PDK and IHP's **open PDK** and GlobalFoundries' 180 nm PDK (GF180) (see also "Open-source PDKs for chip design" information box). However, the open PDKs that are available to date only support more mature technologies with node sizes of 130 nanometres and more. Access to modern fabrication technologies is therefore often denied to small companies and start-ups that have neither large order volumes nor the financial resources to place orders for modern commercial PDKs.

One option for reducing high chip fabrication costs is to place different designs on a single silicon wafer, what is known as a **multiproject wafer (MPW).** A number of developers or companies share a wafer and the individual dies with the **different designs** are delivered to the parties involved after fabrication.

Open-source PDKs for chip design: SkyWater 130 nm GlobalFoundries 180 nm and IHP 130 nm

The **SkyWater 130 nm open-source PDK**[47] was jointly developed by SkyWater Technology with Google. It enables universities and start-ups to gain initial experience in chip design and to develop prototypes at low cost. However, the PDK is limited to 130 nm technologies and is thus more suitable for creating microcontrollers, sensors or mixed-signal designs.

Similarly to SkyWater 130 nm, **GlobalFoundries' 180 nm (GF180) PDK**[48] was jointly published in collaboration with Google. Compared with SkyWater 130 nm, GF180 offers better options for analogue and RF designs, but is not optimised for digital designs.

IHP has also published an **open PDK** for its **130 nm BiCMOS technology.** To date, this is only available as an experimental preview[49] and cannot yet be used for production.

45 | See ETH Zurich 2024.
46 | See https://open-source-chips.eu/
47 | Information on the SkyWater Open Source PDK can be found at GitHub, URL: https://github.com/google/skywater-pdk [as of 29.04.2025].
48 | See GitHub 2025a.
49 | See IHP PDK 2024.

Step in digital design toolchain	Open-source tool
Architecture & system design	SystemC (GCC, Clang), SystemVerilog (Slang, Surelog), topwrap, fusesoc, Kactus, Chisel, SpinalHDL, GHDL, TerosHDL, CIRCT
Synthesis	Yosys+ABC with plugins for SystemVerilog (Slang) and VHDL (GHDL)
Place & route	OpenLane, OpenROAD, padring, Coriolis
Data preparation, sign-off	OpenLane, OpenROAD, KLayout, Magic, CVC
Validation	NetChain, OpenROAD, OpenSTA, OpenRCX, KLayout, Magic, netgen, EQY, MCY, SBY
Design for test	Fault
Verification	Verilator, Icarus Verilog, Cocotb, Surfer, gtkwave, Covered, pyUVM, vUNIT

Table 1: Open-source tools for the digital design toolchain[50] (source: own presentation)

3.1.1 Open-source as an alternative and supplement to proprietary solutions

Consideration of the respective advantages and drawbacks of open-source and proprietary solutions clearly reveals that these two approaches are not in direct competition with one another but that one or the other option makes more sense in certain use cases. While **proprietary tools** are usually ahead of **open-source alternatives** in terms of **performance and efficiency,** using the latter is, for example, subject to **fewer constraints with regard to usage licences.** Open-source IP libraries, EDA software tools or PDKs should thus not be seen as competition to existing proprietary offerings. Instead, they can be considered as a **supplement or alternative** in cases where the use of conventional tools with their economic, legal or technological constraints is not optimal.

However, when using **open-source solutions,** it must be borne in mind that these tools are for the most part **not "turnkey"** solutions for the specific problem, but often have to be configured and adapted for the intended application. In the simplest case, this can be done by the users themselves but from a certain level of complexity it often becomes necessary to rely on service partners who are familiar with the tools.

Once open-source design tools are an essential element of their own chip development work, companies have the opportunity to build up the necessary expertise and resources to maintain these **tools** themselves and **adapt them to their own requirements.**

This is a key advantage over **proprietary design tools,** which always remain in the **possession of third-party companies** which can modify the **terms of use** (e.g. prices) at any time. While using open-source solutions does not necessarily mean reduced costs, it does create independence from proprietary solutions. Other advantages and drawbacks, such as performance, range of features, adaptability and availability of services, must be weighed up depending on the use case. The following section describes and evaluates the situation for open-source IP, design tools for digital (custom design) and analogue (semicustom flow) circuits together with PDKs and ADKs.

Table 1 shows a selection of open-source alternatives to the solutions from proprietary providers for the digital circuit design toolchain. Open-source solutions can, with some restrictions, replace proprietary tools for the exploratory design phase and when more mature technology nodes are used. Current developments are continuously increasing the performance of open-source tools. However, there are also some **gaps in the open-source tool landscape,** in particular in the final steps of the design process, such as *design for test*, for which there are currently no adequate open-source solutions. In figure 6, the areas marked in yellow indicate where open-source design tools are already available, albeit less mature than established proprietary offerings. Steps marked in orange cannot as yet be reproduced adequately or even at all with open-source solutions and it is here that there are gaps that need to be specifically analysed and closed.

50 | The list is intended to provide an overview of common open-source design tools for the digital design toolchain, but makes no claim to be exhaustive. A comprehensive and up-to-date overview of open source EDA tools can be found at https://codeberg.org/fsi/toolchain-directory

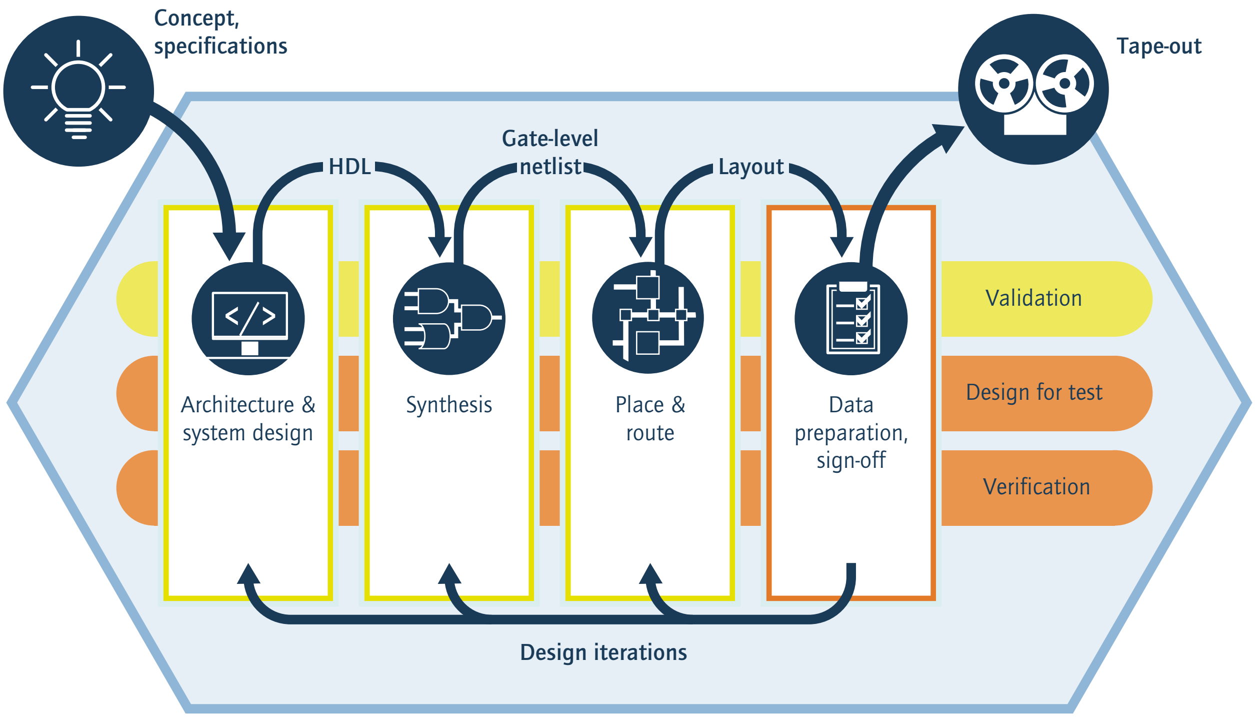

Figure 6: Classification of the maturity and availability of open-source tools for the steps in the digital design toolchain (source: own presentation)

The **FOSSi Foundation**[51] proposes a focus on the following goals for a European semicustom design roadmap[52]:
Short-term goals:

- Improvements in the field of parasitic extraction, including experimental verification on fabricated chips
- Use of open-source IC design tools for advanced technologies
- Support for scan insertion, error analysis and automatic test pattern generation
- Reduction in the runtime of EDA tools for large designs
- Support for multicorner/multiconstraint designs
- New approaches for design for test (DFT) and design for manufacturing (DFM)
- Support for 2.5D and 3D integration
- Creation of synthetic benchmarks for tool calibration and validation
- Improved support for FPGA designs and FPGA-to-ASIC flows
- Baseline SRAM generators for open-source nodes, integration of SRAM generators into the digital design flow (inference)

Medium- to long-term goals:
- Formal equivalence check along the entire digital design flow
- Development of memory controllers for DRAM and their simulation
- Research into ML-assisted methods for the digital design flow
- AI-based physical synthesis and floorplanning
  - design space exploration with ML assistance
  - use of LLMs for assisting with design flow scripts
- Further development of design flow for:
  - multipower-domains, power gating, power optimisation and power delivery networks
  - signal integrity analysis
  - structured placement and routing
- SRAM generators PPA-optimised for smaller nodes

While these steps focus on the technological aspects of the open-source design toolchain for semicustom design, there is also a need for economic and organisational measures in order to achieve the expected benefits of open-source solutions that are described in subsections 3.2 and 3.3 of this publication.

51 | See https://fossi-foundation.org/
52 | See The FOSSi Foundation 2024.

Step in analogue design toolchain	Open-source tool
Architecture, schematic/netlist entry	Python, Xschem, Qucs-S, pygmid
Custom layout design	KLayout, Magic, gdsfactory
Physical verification/parasitic extraction	Magic, KLayout, KLayout-PEX, netgen
Simulation	Ngspice, Xyce, CACE (simulation runner), OpenVAF (model compilation)
Validation	KLayout, Magic, netgen, OpenEMS (EM solver), GAW (waveform viewer), PyOPUS
Design for test	CVC
Final verification & sign-off	Magic and KLayout (parasitic extraction), CACE (PVT, Monte Carlo)

Table 2: Open-source tools for the analogue design toolchain[51] (source: own presentation)

Analogue design/custom design: There are also open-source solutions for analogue circuit design but the design toolchain is less complete here than in digital design. Table 2 shows a selection of common open-source design tools. It is clear that only the first steps in the analogue design toolchain are well covered by open-source solutions. As illustrated in figure 7, there are significant gaps right from the layout phase, where open-source solutions are either not available or have very limited performance and efficiency. The functionality of available open-source solutions is currently inadequate in particular with regard to simulation.

The FOSSi Foundation proposes a focus on the following goals for a European custom design roadmap[54]:
Short-term goals:

- Improvement of open-source EDA tools for commercial use
- Improvement in the quality of existing open-source EDA tools
- Availability of open-source PDKs for analogue design, including advanced SPICE/Verilog-A and EM simulation models and parasitic extraction

Medium- to long-term goals:

- Use of AI/ML in the IC design and verification process: development of AI-assisted methods for optimising and automating design and verification processes
- Performance alignment of open-source EDA with commercial tools
- Development of design tools for THz circuits: creation of specialised tools for designing THz circuits
- Tools for neuromorphic computing and sensor systems: development of design tools for brain-inspired computing technologies, including analogue and digital CMOS designs, memristors, ferroelectrics and stochastic devices on a single SoC
- Development of high-performance analogue generators
- If the design tools are to be a real alternative to proprietary offerings, further development is urgently required, for example as part of targeted funding to give start-ups and development service providers the opportunity to create analogue design business models based on open-source solutions.

Packaging & test: The packaging & test field is largely served by established companies with solutions developed in-house. Since these solutions are tailored to the proprietary design tools' specific requirements and interfaces, with the exception of Open3D-Flow[55] there are as yet no widespread open-source solutions for this field. The APECS pilot line (see box), which is intended to address this issue, is one important activity in this area.

53 | The list is intended to provide an overview of common open-source design tools for the analogue design toolchain, but makes no claim to be exhaustive. A comprehensive and up-to-date overview of open source EDA tools can be found at https://codeberg.org/fsi/toolchain-directory

54 | See The FOSSi Foundation 2024.

55 | See GitHub 2025b.

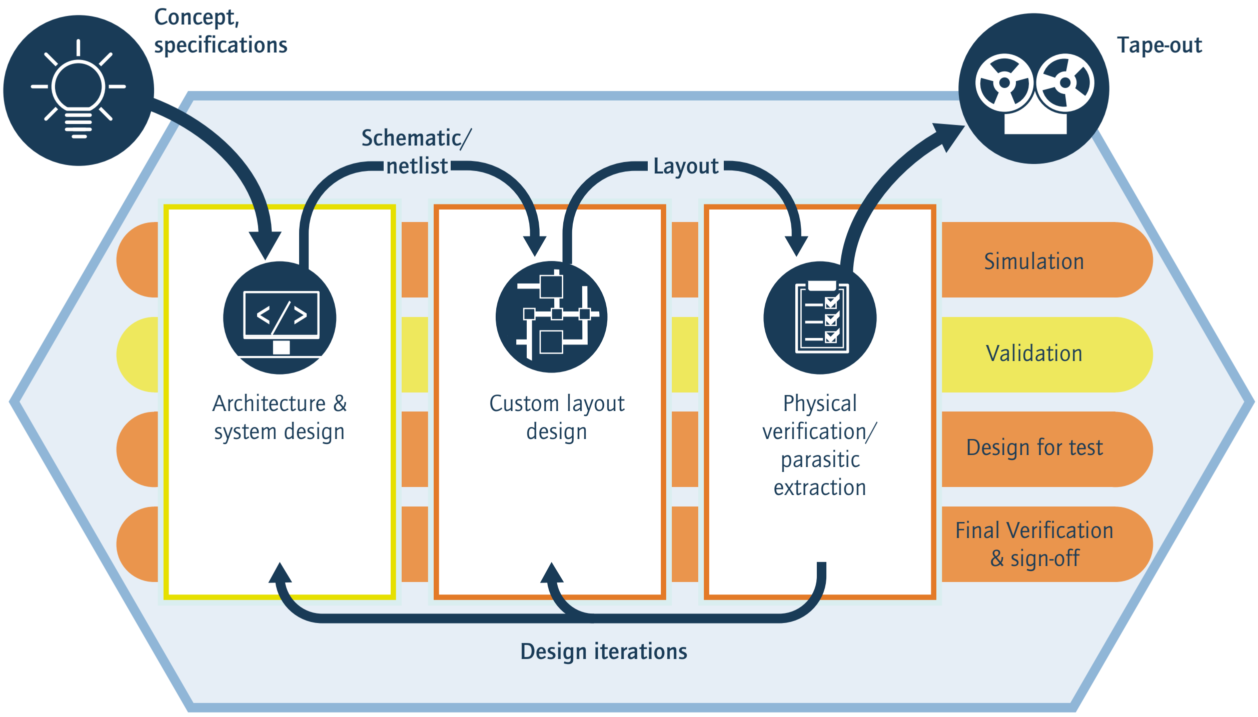

Figure 7: Classification of the maturity and availability of open-source tools for the steps in the analogue design toolchain (source: own presentation)

The FOSSi Foundation proposes a focus on the following goals for a European packaging & test roadmap[56]:
Short-term goals:

- Tools for system-in-package (SiP): need for tools for substrate-based integration of standard dies with a focus on signal delay, thermal management and testing
- Open-source assembly design kits (ADKs): development of open ADKs for heterogeneous integration and packaging pilot lines in the EU

Medium- to long-term goals:

- DFT tools for chiplets: need for specific design for test methods
- Simulation tools for thermal and electrical properties of SiP designs
- System-on-die (SoD) integration: increasing relevance of tools for complete integration of systems on one die in the long term
- DFM tools: long-term development of design for manufacturing tools with physical monitoring and open ADKs for chiplet systems taking account of legal security requirements
- Further open-source PDKs: not absolutely necessary, but beneficial for the integration of proprietary and open-source chips

European APECS pilot line for advanced packaging and heterogeneous integration for electronic components and systems

The APECS pilot line (advanced packaging and heterogeneous integration for electronic components and systems)[57] is intended to expand semiconductor research and fabrication capacities in Europe and spur on **chiplet innovation.**

The pilot line is being set up by institutes and European partners cooperating within the framework of **Research Fab Microelectronics Germany (FMD).** This will pool the technological expertise, infrastructure and know-how of the ten partners – including the Fraunhofer-Gesellschaft as coordinator and the two Leibniz Institutes FBH and IHP –from a number of European countries.

56 | See The FOSSi Foundation 2024.
57 | See Fraunhofer IIS 2024.

APECS is intended to provide not only large companies, but also **SMEs and start-ups** with low-barrier access to the latest technologies. The project is a major building block of the EU Chips Act and is cofinanced with funds from the *Chips Joint Undertaking*[58] as well as national funding from Germany and other European partners[59].

Productivity, interoperability and verification: Strengthening European chip development will require further overarching measures that go beyond the points mentioned and enable greater productivity. New design methods and modern software practices can speed up the design process. Intuitive graphical user interfaces and better documentation promise more widespread use and user-friendliness.

The **FOSSi Foundation** proposes a focus on the following goals for greater **productivity, interoperability and better verification processes** (The FOSSi Foundation 2024):
Short-term goals:

- Design IP management: facilitating the creation of reusable IP through common exchange formats
- Deployable cloud containers: support for continuous integration/continuous development (CI/CD) environments
- Industry-standard verification support: full support for the unified verification methodology (UVM), unit tests (pass/fail), coverage metrics and integration into modern CI/CD workflows

Long-term goals:

- Integration with industry-standard tools, support for domain-specific methods
- More intuitive graphical user interfaces: development of interactive interfaces and improved traceability and communication of design information
- Standardisation of technology files: uniform DRC and LVS rules, device parameters, netlists and pins
- Industry-standard verification support, FPGA-based emulation and verification
- AI-assisted verification: research into the use of LLMs (large language models)

Here too, the goals are of a somewhat technical nature and, in addition to these measures, there is also a need for suitable economic and organisational steps to establish the development ecosystem for open-source design tools as an alternative and supplement to proprietary offerings.

3.1.2 Open-source as an enabler for special applications and future technologies

In addition to their use as an alternative and supplement to established proprietary tools, the second important field in which open-source design tools can offer an advantage is in **special applications and future technologies.** Since the large proprietary design tools are mainly developed for major customers in the USA in line with market requirements, suitable tools are often not offered for new technologies with a still limited market potential and a still small customer base. In these communities, the necessary tools are therefore necessarily developed in-house and, in the case of start-ups and research projects, are usually also made available as open-source. As soon as a tool reaches a significant size in terms of features and users, it is usually bought up by one of the major providers and integrated into their proprietary portfolio, while the open-source version that is still available stops being maintained. Two key future technologies in which open-source development tools are already available are presented below by way of example:

- **Photonic computing:** photonic components are established in communications technology for transmitting large volumes of data around the globe at close to the speed of light. Using established fabrication processes, the focus of research and development is now increasingly moving onto photonic special processors in which, instead of voltages and currents, the properties of light waves are modulated and a number of such modulated signals are combined to replicate computing tasks. Photonic chips are particularly well suited to matrix-vector multiplication, as required for artificial intelligence applications, and have the potential to be used as co-processors for computationally intensive tasks. In contrast with electrons, light particles have many degrees of freedom and so enable simultaneous data processing with comparatively low energy consumption. Since only few design tools are available for this new application, the start-ups active in this field sometimes use available open-source design tools for designing electrical circuits and adapt them to optical circuits.[60]

58 | See Chips JU 2025.
59 | See European Commission 2025.
60 | See Kissner et al. 2024.

- **Quantum computers and sensors:** quantum computers are likewise a completely new approach that opens up new possibilities for data processing that are beyond the capabilities of existing computer architectures. As there are numerous competing technologies and architectures for building quantum computers and it is not yet possible to predict which of these will prevail, we will not explain how these computers work at this point. An overview of current technological development paths can be found in *The innovation potential of second-generation quantum technologies*.[61] The use of tools for automated circuit design will also be necessary for this future technology once a critical level of complexity has been reached. One example of open-source design tools in this technology domain is the Qiskit environment.[62,63]

The two examples outlined above are examples of how open-source design tools can offer an advantage in promising future technologies that so far have neither concrete added value in a defined application nor a functioning business model. While proprietary providers of fee-based design tools for such future technologies would have difficulty attracting customers, freely available open-source tools enable low-barrier access to the technology, so accelerating its development and simultaneously ensuring the availability of specialists trained in future technologies.

3.2 Business and organisational framework for open-source design tools

Open-source denotes a **cooperative development method** that can accelerate innovation (see section 1); business models are created in different phases of the value creation process. Even if the distinctions are not entirely clear-cut, the value creation associated with open-source can, for simplicity, be broken down into **three areas:**

- **Value creation of open-source:** open-source products can themselves, figuratively speaking, be understood as stakeholders. The specific characteristics of open-source products shape both the nature of collaboration between developers and their relationship with the product itself. In the education sector, practical experience in dealing with open source code is in particular seen as a kind of value creation as it can give learners a deeper technical understanding than would be possible with proprietary products.
- **Value creation with open-source:** business models using open-source create commercial value. As enablers, open-source products are not the actual purpose of the business but are merely means for providing an independent service. In the case of chip development by a design house, the business purpose is not open-source design tools, but the chip designs created with their assistance as intellectual property.
- **Value creation by open-source:** if business models are based directly on open-source and value creation is due to the sale of services in connection with open-source technologies, then open-source creates value. Depending on the business model, value creation can serve both commercial interests and public utility in the sense of a commons.

The following subsections explain **value creation of, with and by open-source** in more detail. Different types of value creation are illustrated in information boxes using practical examples.

The first subsection focuses on open-source value creation in **education and research,** taking account of ongoing activities by Chipdesign Germany and other funding initiatives at the national and European level. The second subsection describes the **motivation to make commercial use of open-source design tools.** In this context, the challenges and limitations associated with such use are highlighted in addition to the uses already possible today. Since the goal is a self-sustaining open-source ecosystem, the third subsection finally presents some **possible open-source-based business models,** categorising existing business models and roughly outlining possible development pathways.

3.2.1 Value creation of open-source: better education through transparent structures

Recent years have seen a continuous drop in **student numbers in electronics and electrical engineering** disciplines.[64] In addition to the demanding nature of the subject, one reason for this is considered to be the lack of relevance of the content taught to the digital industry visible in everyday life. While computer science students can, after just a few semesters, put their programming skills to practical use in their own programs and applications for which successful business models may possibly be found, the content taught in microelectronics, in particular in chip design,

61 | See acatech 2020.
62 | See IBM 2025.
63 | See Qiskit Community 2025.
64 | See Statista 2024.

often remains theoretical due to high fabrication costs and large companies offer the only plausible career path for graduates.

While **proprietary design tools** are widely **available** to students under academic licences they can only be used free of charge in an academic context and the circuits developed with them cannot simply be spun off into a start-up. In addition, how the proprietary design tools actually work remains hidden behind the user interface, so preventing independent developments in the field of automated circuit design.

Open-source design tools are one possible solution, where licences are unbureaucratic and inexpensive and mean there is no need for non-disclosure agreements. This significantly lowers the **barrier to entry in education and research** which means that even school pupils as well as students can familiarise themselves with the microelectronics design toolchain.

However, it is not only young people's first contact with microelectronics that open-source solutions facilitate. The experts interviewed also report that, by developing their own chips, students are excited by the subject right from an early stage and gain deep insights into how the technology works through **transparent access to the source code.**

The open-source approach in itself creates value by having a positive impact on the quality of education and contributing to the **formation of human capital.** The transparency of open-source code assists with the acquisition of programming skills and putting this knowledge to direct practical use.

Particularly **outside established markets,** for which there are already proprietary electronic design automation solutions, open-source tools have the potential to support **academic research** and contribute to **spin-offs** from university research. In the absence of licensing restrictions, researchers can adapt the software to their specific needs, develop new methods and share findings directly with the scientific community.

Open-source tools lower the barriers to entry for **start-ups** as there are no high licensing costs to pay during commercialisation and innovations can potentially be brought to market faster.

Chip design at institutions of higher education: the PROGENITOR project

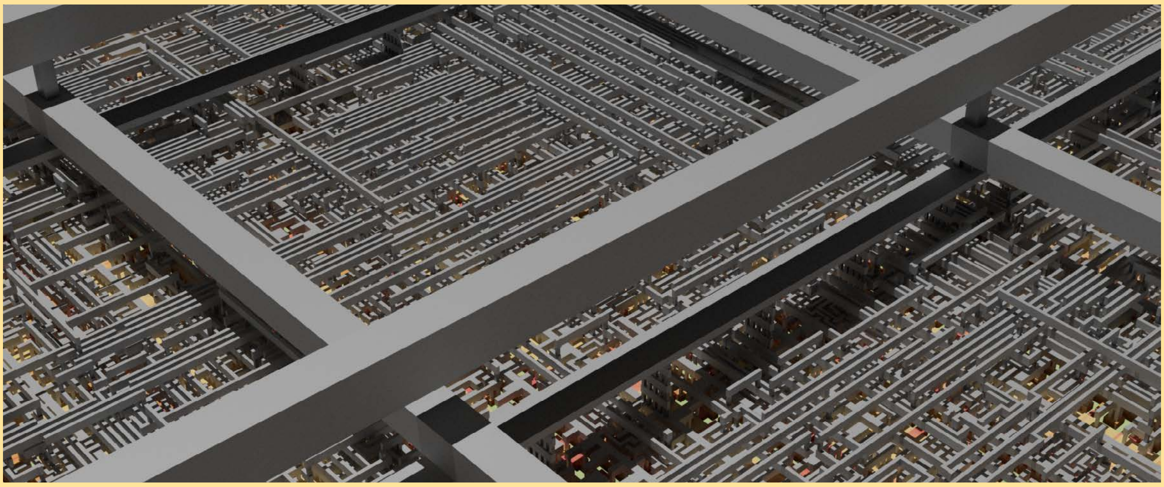

Figure 8: Open-source chip rendering at the RheinMain University of Applied Sciences (source: Daniel Schultz, Hochschule RheinMain; https://github.com/aesc-silicon/i2c-gpio-expander/blob/main/images/chip_logic_closer.png)

A **SoHo WLAN router** was developed as part of the **PROGENITOR** project at the **RheinMain University of Applied Sciences.** Hardware and software were designed in a completely transparent process that included an in-house chip design with its own firmware.[65]

The goal of the project, funded to the tune of **EUR 350,000 by the Hessian Ministry of the Interior and Sport**, was to scientifically investigate and test improved and novel methods for building **electronic network components for security-critical applications** to boost digital sovereignty.[66]

All those involved in the project have positive experiences to report. **Digital sovereignty** starts with the education of young people and projects such as PROGENITOR make the subject visible so young people can be won over to it. The project also shows that your own small microprocessor can be built and taken to the tape-out stage as part of a **practical training** course.

65 | See Hochschule RheinMain 2021b.
66 | See Hochschule RheinMain 2021a.

German and European support for the chip design ecosystem

The federal government has recognised the economic significance of chip design and the importance of open-source design tools and increased support for this field through the **German Microelectronics Design Initiative.**

The Chipdesign Germany network was set up as a central exchange and cooperation platform for chip design stakeholders in Germany. In addition to an open exchange of ideas between all the stakeholders involved in chip design, the intention is also to provide suitable structures for cooperation (for instance a directory of expertise). Consultancy services for start-ups and SMEs and the development of new business models are also planned.[67]

Chipdesign Germany is supported by a **partner network of relevant institutions** including edacentrum GmbH, Research Fab Microelectronics Germany (FMD), RPTU University of Kaiserslautern-Landau, and Leibniz University Hannover (LUH). The Federal Ministry of Education and Research (BMBF) is funding the platform for a period of three years.

In early 2025, the **BMBF** also launched a supplementary **call for projects to close gaps in open-source design tools** as part of the design initiative. Areas to be supported include:

- **completion** and expansion of **open-source design tools and design environments,**
- open-source **data formats** and tools for creating and optimising **PDKs** and **libraries,**
- **verification** and **testing and**
- accompanying **initial and further training programmes.**

In addition to the national programme, funding initiatives are also planned at the **European level** – as part of the **Chips Joint Undertaking** – for an open-source European ecosystem for chip design automation. The following funding priorities have been identified on the basis of the FOSSi Foundation's roadmap:

- **open-source analogue** and **mixed-signal,**
- **productivity, interoperability and verification** and
- **system-on-chip innovation** and open-source **digital chip design.**

3.2.2 Value creation with open-source: motivation to use open-source design tools

The stated advantages of open-source design tools in education and research largely also apply to SMEs seeking an **inexpensive entry into chip design.** However, for most of the experts interviewed, the financial aspect, which can be challenging with proprietary software, is just one of a number of factors which determine the selection of appropriate design tools.

Although only a **few companies** have so far made extensive use of open-source design tools, the following factors that speak in favour of using them were mentioned in the background discussions.

- **Usage or non-disclosure agreements:** it is usual for customers to sign usage and non-disclosure agreements (NDAs) in order to use proprietary EDA tools, IP and PDKs. The terms of use also restrict the creation of open-source IP created with the assistance of these tools.
- **Trade barriers:** in the event of trade conflicts, microelectronics companies dependent on proprietary EDA tools are exposed to the risk of restrictions and far-reaching trade barriers.
- **Asymmetric negotiating power:** prices for design tools are often individually negotiated, with large companies, due to their size and personnel resources, being able to achieve a better negotiating position for favourable terms (discounts of over 90 per cent are not uncommon) than SMEs and start-ups, which often pay annual six-figure sums for single-user licences. EDA companies usually offer their tools

67 | See Chipdesign Germany 2025.

under inexpensive "proof-of-concept" licences to start-ups and spin-offs. However, the full licence costs are incurred retroactively when the resultant chips are commercially exploited and so tie the start-up to the particular EDA company. The resulting high costs require licence management to optimise licence usage.
- **Restrictions on competition:** the publication of performance benchmarks for design tools is contractually prohibited. This is problematic in particular because the underlying algorithms of proprietary EDA tools as well as the information in PDKs are not openly visible. As a result, possible advantages of using alternative tools from other providers cannot be transparently and measurably understood by chip developers so effectively ruling out competition between the various providers. A comparison can only be made if a number of products are purchased at the same time and compared internally. This is also difficult to achieve, especially for smaller players with limited financial and economic resources.
- **Lock-in effects:** since chip development has to be strongly geared towards one of the available tools, changing over to one of the competitors involves considerable effort. In the event of adjustments to contractual terms due to economic or geopolitical changes, the developers are therefore in a poor negotiating position and usually have to agree to the changes.
- **Adaptability for niche solutions:** the market-leading development tools are very much geared towards existing technologies from major semiconductor companies. Current development tools are typically not made for small players or for novel approaches and designs in alternative technology domains. Only once a new technology domain becomes significant do the major development tools offer corresponding functions. Open-source development tools offer an advantage in terms of their adaptability, particularly for universities that are committed to research and development in future technologies. However, they can also be beneficial for start-ups working on non-mainstream technologies that are not yet established.

Despite their stated advantages, open-source design tools are only used selectively, if at all, in large-scale industry as well as in small and medium-sized enterprises (see DECTRIS and OpenTitan boxes). The experts interviewed consider that the following factors explain why reliance is mainly placed on tried-and-tested solutions from market-leading companies:
- **Quality of proprietary tools:** commercial EDA providers continually invest in improving their software and can build on decades of experience. Since a faulty design means high costs due to the complex fabrication process, companies attach great value to proven, mature solutions with guaranteed functionality and minimum risk.
- **Support and maintenance:** while proprietary providers offer comprehensive technical support, regular updates and bug fixes, especially for major customers, the further development of open-source tools currently often depends on a community or a small number of developers. The absence of support can lead to delays and risks.
- **Liability and compliance risks:** companies must ensure that their tools meet regulatory and statutory requirements. With open-source tools, there is frequently no entity that takes care of the necessary certifications. In addition, it is often unclear who is liable in the event of errors or security gaps, which can be problematic in highly regulated industries.
- **Established workflows and investments:** companies have often invested considerable resources into existing toolchains and internal processes. Changing over to open-source solutions can result in high training and migration costs, which discourages companies from switching, or is not even feasible due to lock-in effects. Many external design service providers work with certain proprietary tools and formats. To ensure seamless integration and smooth data exchange, companies stick to the common standards of major EDA providers.
- **Security concerns:** companies fear that the open source code offers potential scope for attack in the form of tampering or IP theft. It is vital to protect intellectual property in particular in security-critical sectors such as the automotive and aerospace industries. At the same time, the open-source community frequently points out that open-source code is more likely to allow careful testing and therefore reduces this risk compared to closed-source code.
- **Semiconductor manufacturer requirements:** foundries publish PDKs that are optimised and qualified for commercial EDA tools. Open-source tools are not directly supported by foundry PDKs.
- **Risk of lower performance and unusable products:** open-source tools with their many fewer resources do not have the same depth of optimisation as proprietary solutions. Inefficient algorithms or missing features can result in designs not achieving the required performance or even not being fabricatable. For complex semiconductor components, the tool costs of proprietary solutions are relatively low in relation to the production costs/risks.
- **Affordable offers for academic institutions:** the EuroPractice platform offers inexpensive access to very powerful proprietary development tools in particular for universities.

Even if most of the experts interviewed do not consider these points to be knock-out criteria, it is nevertheless clear that current weaknesses must be addressed and improved as part of new business models for open-source design tools if they are to gain wider industrial acceptance.

DECTRIS: highly vertically integrated deeptech SME

With its 150 staff, the Swiss company DECTRIS is an established **deeptech SME** that develops and produces X-ray and electron beam detectors for the global market with a very high real net output ratio. The company's products are used in science and industry, including in medical imaging, electron microscopy and X-ray inspection.

All core components, from the microelectronic components to the software, are developed in-house in cooperation with research institutions and industrial partners. **DECTRIS' highly specialised ASICs** enable precise detection with high sensitivity and dynamic range as well as noise-free signal processing.

In late 2024, DECTRIS reported on the successful tape-out of a **110 nm mixed-signal chip** with 10 gigabit transceivers at a developer conference for open-source design tools. **Open-source EDA tools** such as Yosys **were successfully used in the development process.**

OpenTitan project: open hardware development and use of open-source design tools

OpenTitan[68] is a **collaborative open hardware development project** for a trustworthy and open-source **hardware root-of-trust (RoT)** platform. The project is supported by organisations such as Google, lowRISC, ETH Zurich, Nuvoton Technology and Western Digital, who are jointly developing an alternative to proprietary security chips.

A hardware root-of-trust (RoT) is a **specially secured hardware component** that acts as a trustworthy basis for security-critical functions within a system. It ensures that fundamental security mechanisms such as authentication, encryption and integrity checks are carried out reliably.

Collaborating in OpenTitan is not a problem for participating companies as the jointly developed product is **not a competitive differentiator.** The hardware root-of-trust can be implemented in data centres, IoT devices, mobile devices and critical infrastructure. The aim is to ward off attacks on the systems concerned using a chain of trust.

OpenTitan's development process is based on experience from the software sector and transfers proven **open-source principles to chip development.** The project is hosted by the British company lowRISC, which also plays a key role in coordination and further development. OpenTitan demonstrates the extent to which open-source approaches can be used today for developing industrially usable chips.

Since OpenTitan relies wherever possible on open-source design tools, the project simultaneously tests their industrial maturity and reveals the challenges of a **hybrid toolchain of open-source and proprietary tools.**

- **Yosys** is used for generating **netlists,** but primarily for security verification. However, Yosys is not ideally suited to the commercial back-end. Yosys can be regarded as a bridge between innovative academic tools and conventional EDA tools.
- In the **physical security** field, the project draws on scientific findings and makes targeted used of open-source tools for verifying individual blocks at RTL level. **Verilator** is used for simulation, but is not suitable for complete design verification, as certain models cannot be replicated.
- Analogue components are vital to OpenTitan, which further complicates implementation because **proprietary solutions** have to be used. This is a hindrance as the tool's results can then only be **disclosed and disseminated** to a limited extent.

The experience from OpenTitan shows that the available verification tools in the **digital area** from the transition from front-end to back-end are not yet sufficiently mature, while in the **analogue area** essential tools are completely missing.

68 | See opentitan 2025.

3.2.3 Value creation through open-source: commercialisation of open-source design tools

In addition to companies that use open-source solutions as part of their business models, there are also those whose **core business** is the operation of open-source platforms or that offer services in connection with open-source systems.

Open-source systems have established themselves in **software engineering** for professional applications. At the beginning, many companies were sceptical of collaborative open-source software development. Some saw this approach as "cancer" for intellectual property.[69] It was only once commercial business models had become established on the market that the image of this approach improved.

There are often **misunderstandings** in connection with open-source systems because laypeople often use "open-source" as a synonym for "non-commercial". However, successful open-source products, like the Android operating system, can very well be commercial products.

The proper **antonym to open-source is proprietary.**

- Open-source: open-source products allow access to the source code or design plans for an item of software or hardware. Subject to an open-source licence, users can view, modify and redistribute the code.[70]
- **Proprietary:** proprietary software or hardware is provided under a licence that restricts access to the source code or the underlying plans and designs. Modifications or redistribution are prohibited without the rights holder's consent.[71]

As figure 9 shows, in addition to the **"open-source" and "proprietary" axis,** which describes the type of licence and access to the source code, there is also a **second axis** ranging between **"for-profit"** and **"non-profit"**. Individual business models in the open-source ecosystem are often multidimensional as the associated products may frequently be located in different areas.

There may be varying combinations of coordinates along the axes. Open-source solutions may be both commercially for-profit as well as being of public utility and non-profit. The same is true of proprietary solutions, which may be for commercial profit, but also of public utility.

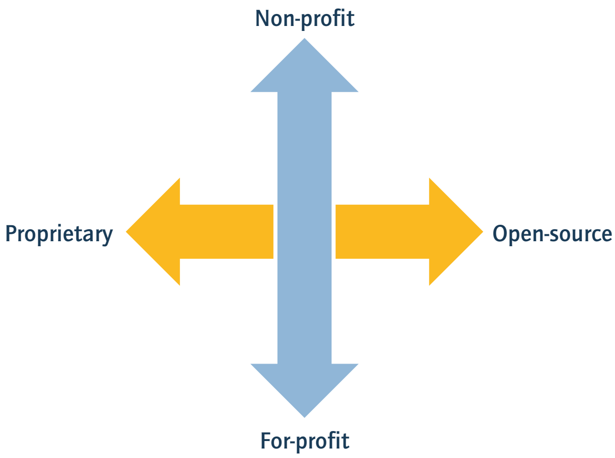

Figure 9: Licence model (yellow) and business model (blue) should be considered separately from one another (source: own presentation)

Whether products and services are made available free of charge is not necessarily dependent on the business purpose. **Organisations of public utility** may also charge a **usage fee** to cover their own costs.

Conversely, there are also commercial proprietary offerings that are, at least with restrictions, free of charge. Similarly to open-source products, such **freemium solutions** frequently have a free basic version to build user numbers and attract them as paying customers for paid add-ons.

Business models for open-source hardware benefit from the, largely transferable, experience gained in the software sector. This is particularly the case for **open-source design tools** for chip design and IP libraries because these, like conventional software, are **intangible products.**

However, unlike conventional software, electronic design automation software is directly intertwined with materials and manufacturing. Design tools for chip design can only be put to productive use if the value chain includes **interfaces** between design tool developers and chip fabs. This means that developers of open-source tools must be integrated into the **semiconductor ecosystem** in just the same way as the developers of proprietary solutions in order to be able to develop marketable products.

69 | See Greene 2001.
70 | See open source initiative 2024.
71 | See Stallman 2024.

If the design tool developer community has sufficient access to expertise from the downstream process steps, there is at least theoretically nothing to stop **business models being transferable** from the open-source side.

For **business models with software-based design tools,** how open-source **licence terms** are structured is of great importance as these terms define how design tools may be used, modified and redistributed.

A very rough distinction may be drawn between permissive open-source licences and **copyleft licences.**

- **Permissive open-source licences** allow unrestricted use, modification and redistribution of the software in both open-source and proprietary projects. They allow developers to choose either to publish their adaptations as open-source or to convert them into proprietary software as they contain no copyleft terms.
- **Copyleft licences,** in contrast to permissive licences, require that modified and extended versions of the software must likewise be made freely available.

While open-source licences are not usually associated with usage fees, **the legal obligations** associated with the licence must nevertheless **be checked and observed.** Start-ups should be provided with assistance with legal issues in order to encourage business models based on open-source tools. According to the experts interviewed, clarification is required about how licences can be purchased, what their use entails and, in particular, how different licences interact and what the effects of this are.

The literature differentiates between seven **archetypal business models** for open-source software. **These models differ primarily in terms of their funding,** their **licence terms** and their **interaction with the open-source community.**[72]

Some of these business models are already part of the open-source EDA ecosystem, while others are merely conceivable. **Table 3** shows a selection of **possible open-source business models.**

Many business models in the open-source sector are **not pure open-source business models,** as revenue is typically generated through exclusive proprietary add-ons. This means that existing proprietary companies and their solutions could well find a place within an open-source design ecosystem. An open-source ecosystem thus always represents a spectrum of different business models. Two different business models are explained below by way of illustration.

Business model	Description
Traditional open-source project	Free of charge publication of an individual project via external platforms such as Github or SourceForge.
Open-source platform	Provision of an open-source platform to attract users and promote network effects.
Donation-based platform	Non-commercial open-source projects based on voluntary work and funding.
Infrastructure business model	Commercial companies that provide infrastructure for a fee. Software offering is available as open-source.
Open innovation	Companies that offer a variety of products/services and focus on promoting open-source innovation.
Open-core platform	Essential functions are open-source, additional proprietary features must be purchased.
Proprietary-like	Proprietary-like platform and infrastructure providers with few open-source offerings.

Table 3: Classification and brief description of various open-source business models (source: own presentation based on Duparc et al. 2022)

A **donation-based business model** is typically free of charge and is supported by voluntary donations and cooperation. In some cases, memberships and advertising generate additional revenue. The product development of non-commercial offerings depends on the cooperation of a broad community. External developers are also taken into account in the decision-making process. “Copyleft” and “permissive” licences provide open contractual terms that are set up to ensure long-term maintenance.

In contrast, **open-core platforms** are distinctly more commercially oriented, which is also reflected in the licence terms and cooperation with the open-source community. Essential functions are open-source while additional proprietary features must be purchased by users. The licences are two-faceted and consist of open-source and proprietary components. There are **freemium models,** which permit basic use for an unlimited period of time, for some of the proprietary features. Cooperation with the open-source community is limited because the latter is not essential

72 | See Duparc et al. 2022.

for value creation. Nevertheless, there are multiple channels to simplify use for external developers.

Profile I: OpenROAD as an example of a donation-based business model

OpenROAD[73] is an academic/industrial non-profit project that has set itself the goal of developing a **fully open and autonomous chip design flow.** It enables the implementation of a digital circuit design from the specification to the finished layout without requiring commercial tools.

The project is led by the **University of California, San Diego** and is supported by companies and public funding. OpenROAD incorporates various open-source tools and algorithms for synthesis, placement, routing, timing analysis and verification.

The platform is helping to strengthen the open-source ecosystem in the semiconductor sector by supporting in particular academic and small industrial design teams working on innovative chip designs. The integration of other projects such as Surelog, Yosys and KLayout facilitates access to design tools.[74]

- **Funding:** combination of government funds (including from DARPA), industry partnerships and membership fees.
- **Licences:** OpenROAD software is published under the BSD 3-clause licence, a permissive, weak copyleft licence.
- **Interaction with the open-source community:** as a non-profit organisation, OpenROAD works closely with partners from the semiconductor industry and academia. Ideas are exchanged via mailing lists and online forums as well as workshops, conferences and webinars. OpenROAD has a clear management structure and strategic decisions are made by a steering committee.

Profile II: YosysHQ as an example of an open innovation business model

YosysHQ is a private company from Vienna that maintains the **open-source synthesis tool** Yosys. Yosys comprises a collection of synthesis algorithms for various areas of application and is the basis for further projects such as Nextpnr, Project IceStorm and Project Trellis.

In addition to open-source solutions, the company also offers **exclusive services and products** that are distributed, for example, as part of the Tabby CAD Suite as a commercial software package. Services include customer-specific developments and training courses.

- **Funding:** grants from (US) authorities, sale of products and services.
- **Licensing:** Dual-licensing model of open-source and proprietary offerings. The commercial component partially cross-finances tool development.
- **Interaction with the open-source community:** close cooperation with academic and industrial partners and the open-source community in research- and development projects.

73 | See OpenROAD 2025.
74 | See OpenROAD Initiative 2025.

Profile III: ChipFlow as an example of an open-core and infrastructure business model

ChipFlow[75] was founded in 2021 with the goal of making cost-effective chip development and fabrication more accessible and flexible without relying on proprietary EDA offerings. This UK start-up offers an **end-to-end platform for chip design** that relies on open-source software and is funded by a wide range of **commercial services.**

- **Funding:** fees for platform use, royalties for IP blocks and technologies and for producing chips based on ChipFlow technology. Subscription costs when using additional features and service costs when using consulting services and individual optimisation and customisation requests.
- **Licensing:** Open-source licensing model for design tools, combined with commercial licences for individual IP blocks and technologies and for using ChipFlow technology in mass production.
- **Interaction with the open-source community:** active cooperation with open-source projects and experts. Integration of open-source EDA tools, such as Yosys and OpenROAD, and redistribution of ChipFlow's own open-source components. Supporting educational programs and close links with universities and research institutions.

Profile IV: Tiny Tapeout as low-threshold access to chip fabrication

Tiny Tapeout is an open-source platform that enables inexpensive and easily accessible production of microelectronic circuits. The project's online infrastructure makes it possible to design and verify a multiproject chip using open-source tools. Each chip contains hundreds of designs that can be activated and tested in succession.

Tiny Tapeout is primarily aimed at students, hobby developers and teachers wanting to gain practical experience in microelectronic circuit design and fabrication.

- **Funding:** the project was partly funded by Efabless, a company which until recently offered an open-source service for multiproject wafers. Thanks to this support, tape-outs could be offered for as little as EUR150.
- **Licensing:** Tiny Tapeout depends on open-source licences to ensure free access to design tools and circuit designs so that all participants can view and learn from the submitted designs.
- **Interaction with the open-source community:** the goal of the project is to lower barriers to chip design. In order to foster inclusivity, Tiny Tapeout actively engages with both newcomers and experienced chip designers, participating in online forums, providing educational resources and offering workshops where developers can share ideas and receive support.

The unexpected closure of Efabless is a major challenge for Tiny Tapeout and the open-source community. Future shuttle programmes with the SkyWater PDK are currently suspended. As an alternative, cooperation with Germany's IHP, which offers a comparable 130 nm process, is becoming increasingly important.

75 | See Chipflow 2025.

3.3 Open-source ecosystems – governance, law and standardisation

At its beginnings in the 1980s, the open-source movement was a small community of dedicated developers. Open-source has now become a central component of the digital world's technological infrastructure. Driven by **new forms of collaborative cooperation** in which the usual boundaries between cooperation and competition have become increasingly blurred, it has fundamentally changed how software technologies are developed, distributed and used.

This demonstrates that technical innovations have an influence on social coexistence, but conversely **social innovations can also be drivers for technical developments.** With regard to the development of generative artificial intelligence, David Donoho explains the meteoric progress that has been made in terms of frictionless reproducibility.

In Donoho's view, the combination of freely **accessible data, simply executable code** for data processing and **competition** is crucial to enabling the numerous parallel experiments, developments and optimisations that increase the probability of technological breakthroughs.

The stated factors are, however, themselves linked to sociocultural conditions.

- The provision of **data may be subject to regulatory and licensing requirements** that determine their use and distribution, for example if the data and the products obtained from them fall within a dual-use context.
- Simple executability of **code** for data processing requires comprehensive documentation, coordinated **standardisation** and **functioning structures for cooperation.**
- Competition within open-source ecosystems must also be supported by business models that adjust their **governance** to this environment. They must strike a balance between economic viability and the common good, between protected unique selling points and shared intellectual property.

If **self-supporting ecosystems** are to emerge, it is not enough to simply promote open-source solutions as an alternative to proprietary solutions. Instead, it is important to improve the organisational, legal and financial framework in such a way that open-source design tools can be used as a strategic advantage and so put to use.

The focus here is on **governance for jointly developed technologies,** for instance to ensure legal certainty and compatibility in commercial applications as part of licensing and compliance initiatives.

Governance, i.e. the **control and organisation of open-source projects,** is explained in greater detail below in connection with the development of open-source ecosystems. Open-source software development and its path from a niche to a global decentralised sociotechnical ecosystem provide the analytical background. Governance is analysed from three different perspectives:

- **Micro level: individual stakeholders**
  social dynamics and an individual's rights and tasks within a project
- **Meso level: projects and communities**
  organisation, structures and decision-making processes within a project or community
- **Macro level: higher-level structures and ecosystems**
  legal framework and the role of norms and standards

3.3.1 Governance at the micro level: individual stakeholders in open-source projects

Governance at the micro level relates to the individual stakeholders and their individual roles within a project. Participants' tasks and contributions and how they collaborate are defined at the micro level. The development of an open-source tool is usually initiated by a person or organisation that has a need for this tool and develops it independently. As soon as the tool is published and meets with a positive response, a community of **users who make use of the tool, report problems and provide feedback** forms, while **contributors** who, thanks to the open-source program code, themselves add **solutions or extensions,** also join. The latter contribute to improving the programs through their involvement, but have no influence on project decisions. A review is carried out before a contribution is accepted.

Once a project reaches a certain size, it is no longer possible for the **owners** themselves to keep track of and incorporate these contributions, so there is a need for **maintainers** who **moderate the community, incorporate contributions** and, in discussion with the owners, **determine the strategic direction of the project.**

As the pyramid of contributors (figure 10) shows, many open-source projects have an additional committer role between the contributor and maintainer levels. **Committers** typically have **no influence on strategic direction, but do have write permissions and can make changes to the program code**[76]**.**

76 | See Bitkom e.V. 2024.

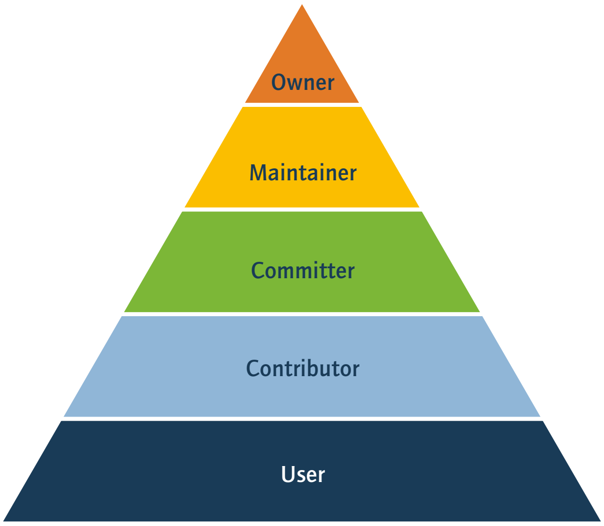

Figure 10: Contribution pyramid of an open source project (source: own presentation)

Governance at micro level thus establishes how decisions are made, who can make contributions to the content of a project and how these are managed. A distinction can be made here between the **"bazaar style"** (e.g. OpenTitan or RISC-V), in which contributions from a broad mass of contributors are encouraged, and the **"cathedral style"** (e.g. the PULP Platform[77]) with a small nucleus of committed contributors.[78] Some projects require contributors to sign a Contributor Licence Agreement (CLA) to ensure that the contributions are used under the relevant open-source licence terms. A usually strict review process guarantees the quality and security of contributions.

3.3.2 Governance at the meso level: organisation and decision-making in open-source projects

The **meso level of governance** addresses **organisational and decision-making structures within a project or community.** The particular form of governance has a substantial influence on how a project can be operated economically in the long term and which business models can be implemented.

Open-source projects usually manage for a long time without formal governance at meso level. However, from a business standpoint, such an informal structure involves imponderables – in addition to dependence on the decision-making power of individuals, the uncertain legal evaluation of open-source projects in particular is a significant risk for companies. For instance, collaboration with other market participants can potentially raise **antitrust issues.**

Even a decision to place an in-house project under an open-source licence is associated with risks from a corporate perspective. This can be counteracted by establishing a **formal governance structure.** Formal governance also reduces the risk of a project being abandoned or not maintained. While open-source licences follow the open-source definition, no fixed rules are defined for governance models. In practice, however, a few – very different – governance structures have become established.

- **"Benevolent dictatorship"**
  control by a central authority – an individual or an organisation – as **owner**. This role often falls to a project's founder and is life-long, which explains the initialism BDFL ("Benevolent Dictator for Life").
- **"Meritocracy"**
  In meritocratic models, control is distributed and awarded in recognition of contributions[79,80]. Contributions are weighted based on the performance and experience of the contributing developers.
- **Democratic models**
  the community makes decisions by voting or reaching a consensus. Democratic governance models are based on joint decision-making, collective responsibility and transparent processes.
- **Company-controlled structures**
  the project is controlled by a company or foundation that then acts as the **owner**.

The governance structure at meso level determines which **business models are feasible** and can be operated sustainably. Corporate-controlled projects have direct potential for monetisation, whereas open-source community-controlled projects, being based on democratic or meritocratic structures, are usually dependent on financial support, donations and funds from charitable foundations.

77 | See ETH Zurich 2024.
78 | See Raymond 2001.
79 | See Ferreira 2022.
80 | See OSSWATCH 2010.

3.3.3 Governance at the macro level: legal framework and role of standardisation for open-source projects

The **macro level** of open-source governance comprises higher-level **structures and ecosystems.** This level considers the influence of larger networks from business and policy making and the significance of standards. While the beginnings of open-source were characterised by collaborative cooperation, today the role of companies, foundations and governments or political decision-makers is becoming increasingly relevant.

- Funding of open-source projects by **governments:** open-source projects receive financial assistance both at the national level, through BMFTR[81] initiatives, and in the context of European programmes. Even countries such as the USA (see OpenROAD information box) and in particular China are fostering the further development of open-source initiatives, often with the goal of achieving technological sovereignty.
- Support for open-source projects by **foundations and organisations:** in many cases, foundations and organisations support open-source initiatives not only by providing funding, but also by assisting with legal issues and structural matters.
- Control and funding of open-source projects by **companies:** large companies such as Google or Microsoft in particular use open-source for strategic reasons in order to accelerate innovation or set standards.

The **legal framework and licence models** are essential open-source governance mechanisms at the macro level. Account must be taken of compliance with **licence terms** when using design tools. In addition to defining conditions of use (including the number of users), these terms determine whether the designs, for example the circuit diagrams and layouts, remain protected by copyright.

Protection of intellectual property also plays a central role in the context of **PDKs. Non-disclosure agreements,** or **NDAs,** protect the information about a foundry's proprietary fabrication processes that PDKs contain. NDAs contain clauses on the protection of intellectual property (IP) as well as design and technology specifications. Design houses must sign an NDA before they are given access to the strictly confidential information contained in PDKs. PDK NDAs usually include a ban on the disclosure of information to third parties, a restriction on the use of the PDK for certain products and staff and the handling of information on completion of a project. Furthermore, penalties are defined for violations of the agreement.

In practice, **NDAs** pose considerable **challenges for start-ups and SMEs,** but also for **universities and research institutions.** As a result, the PDKs from major foundries are often the preserve of established companies that order in large volumes, so making cooperation with them financially lucrative from the foundries' point of view. **Universities** usually receive special **NDAs** which **rule out commercial use.** Experts are also critical of the considerable resources required to complete the processes leading to the conclusion of a PDK NDA. Especially for smaller companies and start-ups, the **legal review** of an NDA is a non-negligible barrier; violations of the provisions set out in the NDA can result in severe penalties, which can have drastic consequences for small companies.

Open-source approaches, such as the open SkyWater 130 nm, GlobalFoundries 180 nm and IHP 130 nm PDKs, offer an alternative (see Open-source PDKs box in section 3.1). In contrast with proprietary PDKs, these are freely available and can be used without concluding an NDA, but have so far been limited to more mature technologies.

Standardisation is another pillar of macro level governance and an essential component of a functioning ecosystem. Norms and standards facilitate collaboration between contributors to different open-source projects by ensuring the interoperability, compatibility and security of different solutions and increasing process efficiency.

- **Interoperability:** standardised interfaces allow different formats and systems to be used and ensure they can work together. New approaches can be more easily integrated into existing products and processes.
- **Resource savings:** the use of common, standardised data formats (e.g. GDSII) and IP block reusability save development time and costs.
- **Reliability:** standards support design testing to ensure the reliability and functionality of the subsequent chip.
- **Security:** standards are essential in security-critical applications to protect against code modification and tampering.
- **Acceptance:** standards foster product sustainability and can thus contribute to greater industrial acceptance of open-source solutions.

Many of the standards of relevance to chip design are **industry standards.** These standards are applied both in open-source projects and in projects and products from proprietary providers. In the electronics sector, industry standards are usually developed in consortia in which numerous well-known companies and tech giants are strongly represented.

The ten defining criteria of open-source

Copyright and patent rights play a central role in chip development. This is particularly the case for design tools which, as software products, are subject to copyright. In most cases, authors assign a large part of the rights, the “exploitation rights”, to their company or customers by contractual agreement. The design tool becomes an open-source tool by the author or exploiter publishing it under an open-source licence issued by the Open Source Initiative (OSI). This requires compliance with the ten criteria of the Open Source Definition (OSD). Design tools available under a certified open-source licence grant users the right to use the tools. **The ten criteria of the OSD** are[82]:

1. **Free redistribution:** the licence shall not restrict any party from selling or giving away the software as a component of an aggregate software distribution containing programs from several different sources. The licence shall not require a royalty or other fee for such sale.

2. **Source code:** the program must include source code, and must allow distribution in source code as well as compiled form. Deliberately obfuscated source code is not allowed.

3. **Derived works:** the licence must allow modifications and derived works, and must allow them to be distributed under the same terms as the licence of the original software.

4. **Integrity of the author’s source code:** the licence must explicitly permit distribution of software built from modified source code. The licence may require derived works to carry a different name or version number from the original software.

5. **No discrimination against persons or groups:** the licence must not discriminate against any person or group of persons.

6. **No discrimination against fields of endeavour:** the licence must not restrict anyone from making use of the program in a specific field of endeavour.

7. **Distribution of licence:** the rights attached to the program must apply to all to whom the program is redistributed without the need for execution of an additional licence by those parties.

8. **Licence must not be specific to a product:** the rights attached to the program must not depend on the program’s being part of a particular software distribution. If the program is extracted from that distribution and used or distributed within the terms of the program’s licence, all parties to whom the program is redistributed should have the same rights as those that are granted in conjunction with the original software distribution.

9. **Licence must not restrict other software:** the licence must not place restrictions on other software that is distributed along with the licensed software.

10. **Licence must be technology-neutral:** no provision of the licence may be predicated on any individual technology or style of interface.

82 | See open source initiative 2024.

By being **members of consortia** in organisations such as **Accellera** (see "Accellera Systems Initiative" box) and of **IEEE or IEC** standardisation committees, companies can **represent their own interests** and **steer technological development.** In practice, this means that major companies exert considerable influence on chip development, determining which specifications, interfaces and formats meet with commercial acceptance.

To counter this trend, some **open-source projects** have **standardised** their solutions and provided them **free of charge,** with examples including the GDSII and LEF/DEF data formats for chip design and also the SPICE simulation program. Further open-source projects offer free specifications for open instruction architectures (RISC-V) or open chiplet interfaces (Chips Alliance AIB).

In some cases, companies also develop their own **proprietary company standards and subsequently** publish them **as open standards** (see UCIe box) to enable collaboration with other companies and solutions.

Defining the market through standards: Accellera Systems Initiative

Accellera Systems Initiative is an independent, non-profit organisation supporting the development of **standards for electronic design automation (EDA) and intellectual property (IP).** Standards and technical implementations developed as part of the Accellera Systems Initiative are incorporated into the formal standardisation processes of the Institute of Electrical and Electronics Engineers (IEEE). Payment is normally required for IEEE standards but they are usually available to students and researchers free of charge via university and library licences.

From industry-standard to open standard: Universal Chiplet Interconnect Express (UCIe)

The UCIe standard was **originally developed by Intel** and was later released as an **open standard.** By defining the interface for chiplets on a package, a number of chiplets from different manufacturers can be integrated as multichip modules (MCM).

In proprietary offerings, the tools interlock seamlessly, while open-source tools usually only cover individual steps in the design toolchain. It is therefore particularly important for **interfaces** to be clearly defined and standardised so that different tools can work together interoperably. In addition to standards, clear documentation of interfaces is helpful for designing compatible solutions (see the recommendations of the FOSSi roadmap in section 3.1).

Developing norms and standards is, however, time-consuming and resource-intensive, both of which constitute considerable obstacles for start-ups and small companies. Targeted support is needed to foster the involvement of these stakeholders in standardisation and so give them an opportunity to help shape the market. Programmes to reimburse the financial expenditure for committee membership together with meeting times and travel could help to broaden involvement by SMEs and start-ups.

4 Applications and specific requirements: current situation and outlook

This section will shed some light on different microelectronics applications and their individual requirements. First of all, subsection 4.1 will assess the German economy's current situation in terms of microelectronics in general and chip design in particular. Subsection 4.2 will describe the benefits and challenges associated with the use of open-source design tools for different stakeholder groups. Depending on the field of application, the purposeful use of open-source design tools may be very beneficial, but there are certain requirements that they cannot meet. Subsection 4.3 expands on the specific requirements and needs of the various applications, and classifies the open-source design tools. The requirements of the applications have led to specific recommendations regarding support for microelectronics, and these are outlined in 4.4.

4.1 Germany, stuck in the mid-tech trap

While other economic areas such as the **USA** and **China** direct massive volumes of **capital towards new, high-growth technologies,** European companies and investors have often tended to concentrate on established markets with lower growth potential.

Germany and the EU are suffering from an innovation deficit, as the continent as a whole has been focusing less on investment in disruptive technologies. However, **productivity gains** are primarily achieved by **disruptive innovative leaps** and not by incremental product improvements. Without sufficiently dynamic innovation in cutting-edge technologies, productivity gains, cost savings and product differentiation fail to materialise, which in turn impedes economic growth and impairs competitiveness[83,84].

The consequence of this **structural weakness** is that Europe is becoming ever **more dependent on non-European technologies and businesses.** If no attempt is made to escape from this mid-tech trap, the European economic area will not only lose technological sovereignty, but also economic resilience against geopolitical uncertainty and trade wars[85].

The mid-tech trap is not so much the result of exogenous factors, such as the war in Ukraine, the protectionist trade policies of major trading partners or high energy prices, as more significantly of a **long-term trend** in politics and business of neglecting, dismantling or indeed relocating cutting-edge technology and investing in it to a lesser extent than comparable economies.[86]

The **loss of technological performance** is insidious, as examples from the electronics industry demonstrate. Nixdorf's demise marked the end of Germany's **computer industry,** while Grundig's insolvency was the final nail in the coffin of Germany's **consumer electronics industry,** and the acquisition of Siemens Mobile by the Taiwanese company BenQ and the termination of Bosch's equivalent business activities brought an end to **mobile radio technology** in Germany and with it the remainder of Germany's consumer electronics. Finally, Siemens' joint venture in **communications technology** with Nokia resulted in the disappearance of the last German provider of telecommunications infrastructure[87].

The loss of this industry means that German industry exerts **fewer pull factors** when it comes to microelectronic components that require particularly intense research and development. The small production runs required by German and European companies in this segment make **scaling more difficult** for European semiconductor companies. As a consequence of the German economy's focus on mid-tech – i.e. on industries situated at a medium technology level[88,89] – there are currently no German or European

83 | See Fuest et al. 2024.
84 | See European Commission 2024b.
85 | See ibid.
86 | See Wagner 2025.
87 | See Hoeffle 2024.
88 | High- and mid-tech industries differ in terms of their R&D expenditure measured as a proportion of sales revenue. The classification used by the ifo Institute Munich, Università Bocconi and Business School Toulouse is similar to that used by Eurostat and the OECD (see OECD 2022). High-tech encompasses aerospace & defence, renewable energies, electronic & electrical equipment, medical equipment & services, pharmaceutics & biotechnology, and software & computer services. Mid-tech covers, among other things, the automotive & parts sector, chemicals, financial services, mechanical engineering and telecommunications services. The "other" category includes, for example, construction & construction materials, the food processing industry, forestry, papermaking, gas, water & multiutility providers, household goods, mining, and oil & gas producers.
89 | See Fuest et al. 2024.

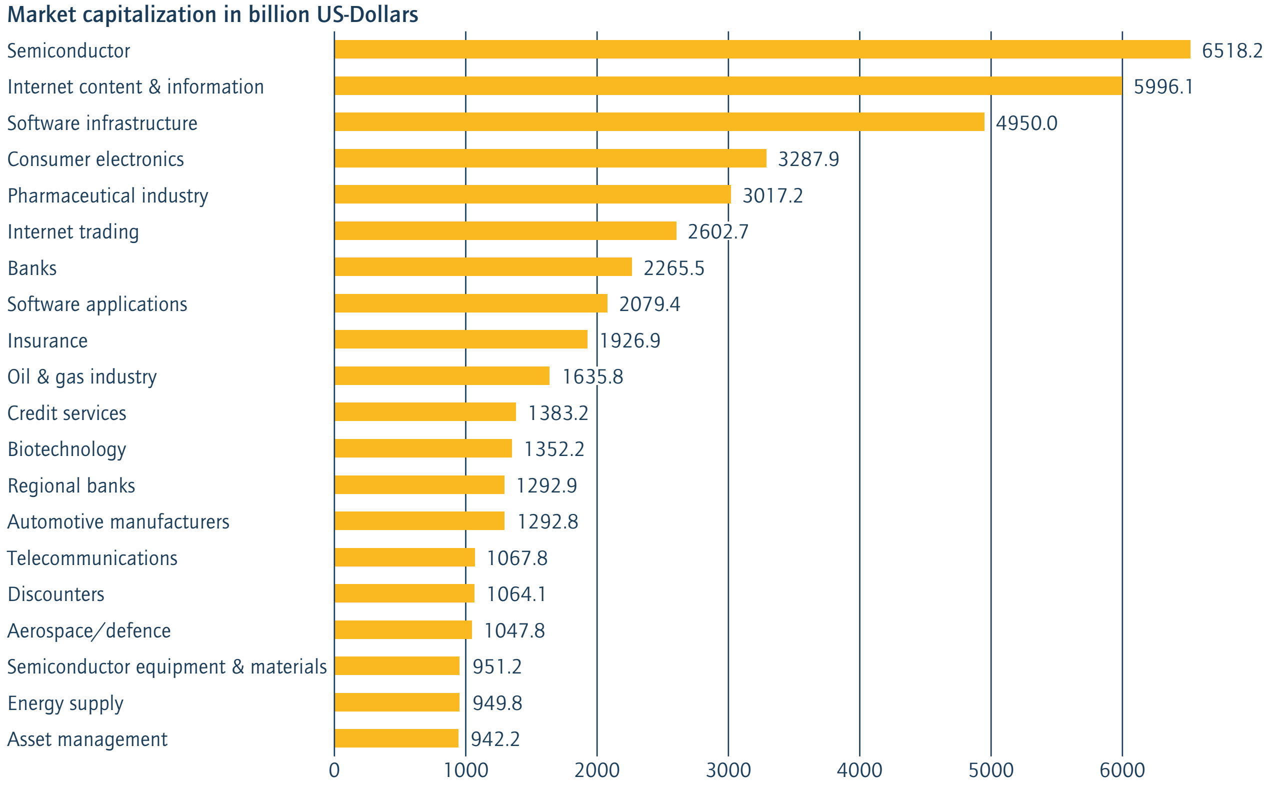

Figure 11: Top 20 most valuable economic sectors globally in 2024 by market capitalisation[90] (source: all electronics 2024)

companies which specialise in chips requiring the newest and most complex manufacturing processes.

The head office of **companies with strong design activities** (Apple, NVIDIA, Qualcomm) and those of the three leading providers of EDA tools (Cadence Design Systems, Siemens EDA, Synopsys) are concentrated in the **USA,** where the macroeconomic focus lies on cutting-edge technology sectors.

On the other hand, **German companies** that develop their own chips are **strongly represented in niche markets** whose products are produced using mature manufacturing processes and are in global demand. However, even these businesses are suffering under the pressure of increasing international competition.

The experts interviewed were of the opinion that **microelectronics continues to be the basic building block of advanced societies** because it is the technological basis for virtually all modern applications. Its importance will only increase in future because it is the driving force behind crucial innovation processes in sectors of the future.

Measured by market capitalisation, the **semiconductor industry is by far the most valuable economic sector** (see figure 11). The stock markets' high rating of the industry reflects the expectation that the greatest **potential for future value creation** lies in technologies based on microelectronic circuits. Industries which supply the semiconductor industry with equipment and materials also have significant value creation potential.

If Germany is to **fully exploit** its traditional **strengths in B2B markets and a strong small- and medium-sized business sector,** then existing **microelectronics-based skills need to be extended and new ones developed.** This applies not only to markets in which Germany is already successful but also to future core semiconductor technologies as a basis for applications in quantum computing, autonomous driving, AI-based robotics or the Combat Cloud for the German Federal Armed Forces and European allies[91].

90 | See all electronics 2024.
91 | See acatech 2024b.

Chip design is a decisive factor when its comes to user industry competitiveness: only through continuous innovation in this field and a **higher real net output ratio can trade advantages be ensured** and high profits achieved.

In the long term, **open-source chip development tools** could play a key role in enabling in particular **SMEs** to develop their own **chip design expertise.** Open access to these resources and their flexibility and adaptability could give companies the opportunity to innovate for themselves, irrespective of the tools that are currently available. Open-source design toolchains for more mature technology nodes hold the promise of strengthening Europe's technological sovereignty and so providing a better cushion against economic and geopolitical threats.

4.2 Different stakeholder types and their respective potential in terms of open-source design tools

It is clear from the analysis in section 3 that there are various reasons why open-source design tools might be attractive to different stakeholders in the microelectronics sector. The typical advantages and challenges for the stakeholder groups science and research, major industry, research services/development providers, SMEs and start-ups are described and analysed below.

Science and research are traditionally very interested in open-source solutions because they provide free access to knowledge and technologies, which is the very basis of independent research activities. Open-source also enables free dissemination of research results and their joint further development, and the transparency of such solutions improves the reproducibility of scientific results, which is crucial to the validity of research. Another advantage is that open-source solutions are freely available, meaning that neither licence costs nor terms of use have to be taken into account.

The **long-term funding and maintenance** of these solutions does pose a **challenge,** however. Open-source projects need continuous development and maintenance, but research funding programmes tend to be project-based and to run out after a few years, with the individuals entrusted with such projects moving on to other projects or moving across into industry. It can also be difficult to obtain acknowledgement for open-source work in scientific career systems, as greater weight is often placed on publications and patents than on contributions to and maintenance of open-source technologies. Maintenance is particularly onerous for microelectronics design tools, with their high level of complexity and elevated quality requirements in practical use, and this often makes the mature development tools provided by proprietary vendors, which are readily accessible due to academic licences for science and research, the simpler option when it comes to rapidly achieving good results. Currently, **both open-source and proprietary design tools are used** in science and research, depending on the individual field of application and the preference of the researchers involved.

For **major industry, open-source tools** offer **the possibility of reducing licence costs on the development side,** since, where open-source IP resources are available, companies can save on costs by using them for technologies which are not differentiators. The availability of open-source alternatives **reduces dependency on proprietary vendors**, which is advantageous in terms of negotiating licence costs and long-term planning. At the same time, large companies can use open-source approaches to develop their own ecosystem perfectly tailored their requirements.

The biggest **challenge** for major industry is the **maturity level of open-source solutions.** Since the semiconductor development chain is highly complex and sensitive to disruption, there is reluctance to risk changing over to an alternative development chain due to the danger of incorrect tape-outs, in particular if a company has little experience of using the tools. The **legal situation may also be uncertain,** especially in terms of licence models and liability issues, but also in terms of the **certifiability** of open-source tools and of the chips and end products developed using them. A further challenge lies in integrating open-source solutions into existing, generally proprietary development environments. Last but not least, the use of open-source solutions generally requires adaptation to internal procedures, which may be associated with high costs and organisational resistance.

Because of these risks, open-source design tools are currently only suitable for major industry at the predevelopment stage – to be suitable for mass production open-source tools would have to display the same levels of quality, reliability and support as proprietary vendors can offer.

Research services and development providers benefit from open-source technologies through greater ease of access to open technologies and the absence of licence costs. Pre-existing open-source components can be reused, so reducing development times and costs for customer projects. Moreover, by actively participating in open-source projects, these service providers are able to position themselves as pioneers in specific technological fields and further develop their technical expertise. The transparency of open-source developments additionally creates customer confidence, as customers can replicate the code and development stages.

The greatest **challenge for service providers** consists in establishing a **sustainable business model** around open-source, as not only customers but also competitors have permanent access to the same tools and also have the option of poaching specialist personnel. Open technologies may thus result in businesses focusing more on their own development resources, rather than contracting out to external service providers. A further problem when it comes to customer requirements is **lack of certification:** research services and development providers have to align with customer specifications, even if they are in principle open to using open-source design tools.

For **SMEs,** it is strategically important not to be dependent on a small number of large providers, making open-source technologies an attractive alternative. They may benefit in particular from **the cost-efficiency and flexibility of open-source solutions,** as they tend to be in a weak negotiating position with regard to the large, established providers and cannot benefit from the deep discounts that major companies manage to negotiate. In contrast, open-source solutions don't have the associated high licence costs, while at the same time the development tools can be individually adapted in order to develop differentiated products for specific market segments.

The greatest **challenge** for SMEs is their **lack of internal resources and know-how. Using and adapting open-source solutions is complicated and requires specialised technical knowledge,** which is something small businesses often lack. In addition, there is uncertainty around the long-term availability and maintenance of open-source projects. Many SMEs therefore shy away from the risk of adopting a solution for which no support is available. It may additionally be problematic for SMEs to use open-source solutions for security-critical or highly specialised microelectronics applications, since many such tools do not go through the same certification schemes and validation procedures as proprietary solutions but these are a customer requirement. For these reasons, open-source solutions are as yet only very little used by SMEs. In particular, the small number of specialised personnel qualified to use and adapt open-source solutions to SMEs' own requirements works against this solution and makes proprietary vendors the only option.

Like SMEs, **start-ups** derive great benefit from the low costs involved in using freely available tools and libraries, with these often being the only way initial prototypes and demonstrators for further funding rounds can be developed in the first place. Open-source communities play an important part as opinion leaders, bringing together new players in a specific application. Start-ups that develop their own open-source solutions can position themselves as technology leaders while simultaneously benefiting from further development by a wide open-source community.

The challenges are comparable to those for SMEs, but often even more serious. Because of the associated costs, the adaptation of open-source tools to a start-up's own requirements has to be learned and managed by that start-up itself, which may distract from development of the actual product. It is difficult to develop a workable business model when using open-source solutions because investors often expect clear protection of intellectual property and therefore the use of open-source solutions has to be combined with a convincing business model. Nevertheless, it is start-ups which make the greatest use of open-source solutions, in particular because most founders come from a research background and can apply the concepts developed there using open-source design tools directly to their start-up without having to overcome financial and licence-related hurdles.

4.3 Concrete applications and their specific requirements

In addition to analysing the various stakeholder groups, it is also worthwhile taking a separate look at the applications that are important to Germany, and these are briefly described below.

Industrial electronics, industrial metrology and Industry 4.0 are key applications for Germany as a place to do business. In addition to large corporations such as Siemens, there are numerous small and medium-sized companies that are technology leaders in their niche markets. Industry 4.0 is opening up huge potential through connected, automated systems, for instance in fields such as robotics or digital twins. These technologies enable more efficient production processes and greater flexibility. Despite its higher costs, German industry remains competitive thanks to its quality leadership, but is under constant pressure from global competition.

Telecommunications have become an indispensable technology in both professional and private contexts. While German players have withdrawn from the consumer market in recent decades, there is still a great deal of expertise in important domains such as radio-frequency technologies and silicon photonics. These are the foundation for resilient and secure network infrastructure solutions for wireless, 5G and 6G. Germany is not, however, the driving force behind new technologies such as global satellite communication for terminals[92].

When it comes to **education and research,** Germany is well positioned relative to international competitors at least in some areas; there is also extensive basic academic knowledge in chip design. However, this knowledge is at risk as many experienced professors and specialists are about to retire, while student numbers in electrical engineering are also falling. This is resulting in a shortage of the specialised personnel who are urgently needed for circuit design and new semiconductor-based applications. One peculiarity of the academic environment is that although academic licences for proprietary chip design are very inexpensive, in the event of new designs being spun off from academia, retroactive licence costs can be charged for commercialising them. Some experts are of the opinion that this can hinder the transfer of research results into industrial use.

Computing and data centres are becoming increasingly important due to increasing digitalisation and connectivity. In particular, increasing use of artificial intelligence, for instance for generative models, is driving up demand for specialised computing power. At the same time, the sector is facing the challenge of managing high energy consumption efficiently and responding appropriately to geopolitical tensions. As Moore's law is reaching its physical limits, alternative architectures such as multicore approaches and special processors are already common, but new technologies such as analogue computing, optical computing or quantum computing are also gaining in importance. New technologies and innovative computing and system architectures in particular have the potential to break down US dominance.

High-quality semiconductor components are essential for reliable avionics, communications and sensor technology in the **aerospace industry.** While Germany's market leader has largely given up on in-house chip development, there are numerous technology leaders in SMEs that specialise in particular applications and are internationally competitive thanks to their quality despite relatively high costs. In the space sector, however, this position is being put at risk by strong growth in private US providers and their market power, as increasing use is being made of selective tenders specifying that "Made in USA" components be used wherever possible.

The **defence** sector is closely linked to the aerospace industry, but has different requirements in terms of security, reliability and durability. Against the background of a global security situation that was perceived as largely manageable, recent decades have seen innovation stagnate. Long delays in development projects were tolerated despite military equipment being two to three generations behind the international state of the art and new developments sometimes being ridiculed as "90s technology" in global comparison. However, the Russian war of aggression in Ukraine and the technologies used there have prompted a rethink and policy makers have recognised the need for investment in modern, powerful semiconductor solutions for communications, radar and defence systems.

High-precision, miniaturised and connected yet intuitively operable systems are required for **medical technology and laboratory automation.** In imaging (e.g. CT, MRI), semiconductor detectors ensure improved signal quality and faster diagnosis. Lab-on-a-chip systems use microfluidic semiconductor structures for automated analyses, for instance in DNA sequencing or point-of-care diagnostics. These applications require high sensitivity, reliability and biocompatibility. At the same time, everyday clinical practice demands compact, integrated designs allowing easy handling. IoT and AI connectivity offer the potential for smart, connected systems that enable accurate, automated and personalised medicine that is nevertheless cost- and resource-efficient.

The **automotive** sector is one of Germany's most important industries and is currently undergoing a transformation away from purely electromechanical to highly digitalised products[93]. Vehicles are increasingly being designed as "computing and data centres on wheels" with standalone systems using simple control devices more and more being replaced by an integrated zonal architecture that demands high levels of computing power. This transformation is being driven by greater use of powerful assistance systems, some of which require edge capabilities. At the same time, the transition from fossil fuels to electrical drive systems is also taking place, which requires a large number of additional electronic components, for example for battery management. The sector is, however, facing rising costs and economic challenges as the strong position of German car manufacturers is under great pressure internationally.

Environmental monitoring makes use of semiconductor technology to acquire environmental parameters such as air and water quality, temperature and radiation. Semiconductor-based sensors (e.g. MOS gas sensors, MEMS sensors, electrochemical detectors) enable high sensitivity and selective measurement. The sensors have to be robust, stable over the long term and energy-efficient in order to be able to work reliably even in remote areas.

92 | See Handelsblatt 2025b.
93 | See acatech 2024a.

Miniaturised systems with integrated sensor electronics and IoT connectivity enable real-time monitoring and smart data processing. Advances in nanotechnology and AI are improving sensitivity and signal processing, enabling more precise and sustainable environmental analyses.

Different applications place **different demands** on the semiconductor elements. The specific requirements have an impact on selection of the design tools used and the advantages and drawbacks of open-source tools compared to solutions from proprietary providers come into play here. The experts interviewed confirm the advantages of open-source solutions under the following conditions.

- **Low-volume production**: while the fabrication process for semiconductor components is designed for very high volumes, some applications only have a small-volume market.
- **High degree of specialisation**: many applications require highly specific solutions that have to be custom-developed and cannot be purchased commercially.

The high costs and lack of adaptability of proprietary design tools make their use less advantageous under these conditions and favour the use of open-source solutions. Providers of proprietary design tools also focus on the major players of the semiconductor industry, which is why open-source solutions are an alternative for SMEs and start-ups in particular.

Conversely, there are conditions that favour the use of proprietary design tools.

- **High innovation and cost pressures**: the global nature of the semiconductor market means that high innovation and cost pressures prevail in most industries, which is why companies stick to proven, widely distributed design tools instead of risking any change.
- **Certifiability**: particularly security-critical applications have stringent certifiability requirements that open-source design tools do not as yet meet because such functionality is not needed.
- **High computing power and energy efficiency**: powerful design tools are indispensable in applications where high computing power or elevated energy efficiency are critical. Proprietary design tools that have been developed at great expense are usually ahead of their open-source alternatives.

4.4 From push to pull: market-driven innovations for chip design tools by user industries

Germany's federal and state governments have recognised the paramount importance of microelectronics to the country's industrial future. The **resolution paper of the Ministerial Conference of the Federal States** in March 2025 holds out the prospect of targeted funding for new chip design architectures[94]. In March 2025, the Federal Ministry for Economic Affairs and Climate Action **(BMWK)** and the Federal Ministry of Education and Research **(BMBF)** also announced that they consider chip design and the advanced packaging sector to have decisive impact potential for technological sovereignty and therefore also for government research funding[95]. In addition, again since March 2025, Germany, following the initiative by the Netherlands, has been a member of a **European "coalition of the willing"** with the aim of strengthening Europe's sovereignty in microelectronics[96].

The stated papers demonstrate that there is support at all political levels for an **attempt to escape from the mid-tech trap.** Especially against the backdrop of the tense geopolitical situation and Europe's need for sovereign solutions to ensure defence capabilities, the aim is to quickly translate applied semiconductor research and development into marketable products.

Economic development initiatives, in particular with regard to SMEs and open-source design tools, should therefore be linked to the specific needs of user industries. This entails a **partial shift away from the push principle,** in which ministerial bureaucrats set the agenda for innovation within the framework of calls for tender, towards **pull mechanisms,** in which the priorities for research and development expenditure are geared to the actual needs of the user industries.

94 | See Sächsische Staatskanzlei 2025.
95 | See BMWK & BMBF 2025.
96 | See Government of the Netherlands 2025.

5 Findings and policy options

At the present time, open-source design tools are not an alternative to established **proprietary solutions** for companies in the German semiconductor industry. Almost the entire semiconductor industry is critically **dependent on a few providers.**

If **open-source solutions** are to gain more widespread acceptance and reach industrial maturity in many applications, some **parameters** need to be adjusted.

- **Open-source EDA tools:** at present, industrial usability is limited by a lower level of technical maturity, a restricted range of functions, limited certifiability and low availability of PDKs.
- **Proprietary providers:** proprietary sellers' established flows lack open interfaces. However, these are a prerequisite for smooth integration and for hybrid design toolchains that include both proprietary and open-source solutions.
- **Design houses, foundries:** there is currently a lack of support for user industry companies with an interest in accessing chip design with open-source solutions.

Despite the stated limitations, open-source tools can already be a profitable alternative for companies **in early development phases** because it is at this stage that the advantage of flexible modifiability is seen as very valuable and there is time to incorporate and customise the tools. It may also be possible to network within the open-source community, for example to identify specialist experts.

Open-source solutions can also be a good option in **education and research** and, depending on the use case, in start-ups and SMEs. In addition to flexible modifiability, the financial and legal frameworks are also a significant advantage here. Moreover, an active **exchange of ideas with the open-source community** can lead to new approaches and innovations.

In **school education,** formats based on open-source design tools and appropriately designed fabrication programs can help to shed light on a subject that is currently under-represented in traditional curricula. This can enable particularly interested pupils, and thus potential students, to engage with the subject without bureaucratic hurdles.

Open-source chip design tools as an alternative to existing offerings can help to secure **technological sovereignty** and boost innovation capacity in particular in forward-looking fields such as optical computing, quantum computing and advanced packaging. A European ecosystem for chip design software could also **keep the added value,** which currently disappears to the USA in the form of high royalties, **within the European economic area.**

However, due to the strong market position and the lock-in effects of the widespread proprietary tool chains, **open-source solutions** require further **institutional support** to reach **industry maturity.** The following policy options are set out below with the aim of enabling movement towards the vision of an industrially mature design toolchain based on open-source tools.

5.1 Policy options for academia

1. At **university level, both proprietary and open-source approaches** should be presented and their respective advantages and drawbacks clearly demonstrated. This would make graduates aware of the issue and might help to break down the often pervasive conviction in companies that there is no alternative to proprietary design flows and so stimulate the ecosystem of existing design tools.

2. Retirements in the coming years will lead to a considerable loss of expertise in the field of automated circuit design. This is happening at a time when chip design is becoming increasingly important and the industry is undergoing profound structural change. As part of a **portfolio process** called for by the Commission of Experts for Research and Innovation (EFI)[97,98] and the Future Council of the Federal Chancellor, the federal states, together with university management, should review the number of appropriate university positions with regard to structural change and use any freed-up capacity to **expand microelectronics.**

3. As in artificial intelligence, Humboldt Professorships could be put to strategic use as a tool to attract international top talent to Germany. In addition, some leading locations in Germany should be set up to be **internationally competitive** in terms of personnel and material resources, taking top public universities such as the University of California, Berkeley, ETH Zurich or the University of Cambridge as inspiration.

97 | See Expertenkommission Forschung und Innovation 2025.
98 | See acatech 2024b.

4. Universities and institutions of higher education in the applied sciences should ensure that existing know-how is maintained and further developed through new professorships and active participation in open-source circuit design projects, as well as encouraging spin-offs. One important factor here is **to make deliverables and results** from funded projects **available in open-source form and defined formats,** which is often not permitted with proprietary solutions due to the licence agreements. Once established as institutional academic practice, this would allow the mechanisms of frictionless design described in section 3 to be set in motion for microelectronics, so stimulating research into automated circuit design and microelectronics as a whole.

5.2 Policy options for industry

1. An **open-source EDA user forum** could be created as a central clearing house between user industries and the open-source EDA community, which includes university groups, non-university research institutions, development service providers and freelance developers. The purpose of such an industry-funded user forum would be to specifically drive forward the development of open-source design tools. The direct exchange of ideas between developers and users could foster the development of common standards that enable seamless integration into industrial development processes. Working groups and regular meetings of the forum would ensure that real-world requirements are taken into account at an early stage and that developments are steered in a direction that promotes long-term industrial use. In addition, close cooperation with institutions of higher education would assist in adapting training content to current technological challenges so that graduates are better prepared for industry requirements. This format would support a market-driven economic and technology policy which, crucially, must be embedded in a long-term semiconductor strategy that regularly evaluates all funding initiatives and makes targeted adjustments where necessary.

2. Although open-source tools are not usually an option for marketable semiconductor products, they should be considered as a supplement and alternative to proprietary tools, for example in early development phases. They are also a valuable option for special applications and future technologies for which proprietary offerings are not available or are not fully mature. Open-source tools are also developing rapidly and could soon become industrially relevant and those companies that **build up early expertise** will enjoy a competitive advantage. Against the backdrop of prevailing lock-in effects, active participation in the further development of open-source alternatives can, at least in certain areas, help to reduce dependencies and improve the negotiating position with proprietary providers.

3. When selecting chip design tools, companies **should give preference to tools which support open standards for input and output formats** and thus ensure compatibility with open-source tools or solutions from other providers.

4. In the case of **solutions developed in-house** and in cooperation with institutions of higher education or start-ups which complement proprietary design tools, it should be checked whether these can beneficially be **shared** with the **open-source community.** In addition to providing impetus for the further development of the solution, cooperation with open-source communities could give rise to new business models, for example based on technical support.

5.3 Policy options for policy makers

1. If open-source solutions are to be usable by companies, support and maintenance must be provided along the tool chain. Should the ongoing activities of the EU Design Platform and the centres of expertise of the EU Chips Act be insufficient, an organisation with appropriate technical and human resources could perform this role at national level. The vision should be a **platform which, as a marketplace or "one-stop shop",** offers not only coordinated and seamless open-source tool chains that are available both online and offline, but also various tape-out offerings. This should be available to all players from academia and industry, both as providers and customers, and would make it possible to break down the proprietary tool chain's prevailing lock-in effects. For companies wishing to share their in-house developed solutions with the open-source community, the "one-stop shop" would provide a trustworthy platform for long-term maintenance. This organisation could also be responsible for the integration of new solutions and further development of existing tools.

2. Behind the scenes discussion with experts from user industries have shown that, in all the sectors considered, German industry is investing only cautiously in in-house chip development. The few companies that are developing chips in-house are primarily relying on proprietary design tools, as they are

wary of threats to their core business related to open-source solutions. Sponsored **EDA development vouchers** could be a way of incentivising the use of open-source design software for design automation and encouraging its further development in line with industry standards. Companies could then apply for funding by stating a use case. The voucher would enable companies to award a contract for the further development of a specific open-source EDA tool to make it industry-ready for their specific use case. As a funding condition, all developments financed with the voucher would have to fall under an open-source licence. The voucher funding mechanism would ensure that the further development of EDA development tools precisely meets the needs of the industry. The vouchers could strengthen the industrial user base and furthermore contribute to a self-supporting ecosystem in the long term.

3. The German semiconductor industry would greatly benefit from a **seamless** open-source **development chain** that is geared to two nodes, for example **22 nm at GlobalFoundries** and **130 nm at IHP.** This infrastructure could accelerate innovation, facilitate access to modern fabrication technologies and strengthen Germany's technological sovereignty. Policy makers should therefore provide targeted funding for this development, for example in the context of calls for tender with a focus on technological implementation, and initially drive it forward at national level to enable rapid availability.

4. **Public funding** for the development of design tools could, where this makes sense, be **contingent on open-source publication of the project results.** However, exploitation interests and possible dual-use risks should be taken into account and weighed up.

Glossary

ADC (analogue-to-digital converter): a circuit that converts analogue signals (e.g. voltage) into digital values. ADCs are used in sensors, audio processing and communications technology.

ADK (application design kit): an extension of a PDK that contains design tools, libraries and additional models specifically tailored to an application. ADKs help designers to efficiently develop complex chips for specific markets (e.g. automotive, IoT).

Analogue design: the design of analogue circuits that process continuous signals, for example amplifiers, oscillators or voltage regulators. Analogue design requires detailed modelling of transistor characteristics and parasitic effects.

ASIC: (application-specific integrated circuit): a customer-specific chip that is optimised for a particular application. Unlike an FPGA, an ASIC is no longer programmable after it has been fabricated but is more efficient and consumes less power.

Chiplet: a small, self-contained semiconductor element that can be combined with other chiplets to form a complete system. This technology makes it possible to implement different functions on separate dies and connect them via advanced interconnect technologies.

Chips: integrated circuits (ICs) that consist of numerous electronic components such as transistors, resistors and capacitors. They are the cornerstone of modern electronics and are used in computers, smartphones and many other devices.

CI/CD: (Continuous Integration, Continuous Delivery): A common practice in software development in which new features are continuously made available to customers.

CMOS: (Complementary Metal–Oxide–Semiconductor): Semiconductor devices in which both positively and negatively doped channels are used on a common substrate

Custom layout design: manual design of circuits at the transistor level to maximise performance and efficiency, often used for high-speed or analogue circuits.

DAC (digital-to-analogue converter): a circuit that converts digital signals into analogue voltages or currents. DACs are essential for audio output, communications and control technology.

DARPA (Defense Advanced Research Projects Agency): a US government agency that develops innovative technologies for military applications. DARPA has sponsored numerous breakthroughs in semiconductor technologies, including early developments in microprocessors and advanced chip design technologies.

Data preparation: the process of converting the chip layout into a format-compliant design for fabrication, including mask layout, optical proximity correction (OPC) and the generation of lithography exposure data.

DFM (Design for Manufacturing): This term describes the general practice of designing products so that they are easy to manufacture. In semiconductor manufacturing, the reduction of defective dies is an important aspect.

DFT (Design for Test): In microelectronics, the manufactured dies must be extensively tested. To make this easier, additional elements are integrated into the design, which are only used for testing.

Die: the actual silicon chip obtained from wafer fabrication. A wafer contains a number of dies that are singulated and further processed (e.g. packaged) after fabrication.

Digital design: the field of chip design that deals with the development of digital circuits, including logic gates, processors, memory and digital signal processing. Hardware description languages (HDLs) such as VHDL or Verilog are often used to carry out digital design.

DRAM (dynamic random-access memory): volatile memory that stores data in capacitors and has to be regularly refreshed. DRAM is the main memory in computers and provides a high storage density.

DRC (Design Rule Check): A work step in chip design in which it is checked whether the design rules of the Fab, such as the minimum track spacing, are adhered to.

EDA (electronic design automation): the use of software tools to assist the design of integrated circuits (ICs). These tools help with schematic design, simulation, verification, placement, routing and production of the chips.

Fab: semiconductor fabrication facility in which microprocessors, memory chips and other integrated circuits are produced.

Floorplan: an early step in the layout process that defines the rough placement of a chip's main components. The goal is to obtain an efficient arrangement that minimises signal propagation times, energy consumption and space requirements.

Foundry: a company that produces chips for third parties without developing its own chip designs. Examples include TSMC, GlobalFoundries and Samsung Foundry. Foundries manufacture ICs on the basis of design specifications from fabless companies.

FPGA (field-programmable gate array): a reconfigurable chip whose circuit is programmable after manufacture. FPGAs are used for prototyping, specific acceleration tasks and customisable hardware solutions.

Gate (logic gate): the basic building blocks of digital circuits that perform logical operations such as AND, OR and NOT. They consist of transistors and determine how a digital circuit behaves.

IC (integrated circuit): a semiconductor element that integrates a large number of electronic components (transistors, resistors, capacitors) on a single chip. ICs are the basis for almost all modern electronic devices.

IoT (Internet of Things): The Internet of Things describes the concept of many everyday devices connected to the Internet, which is intended to enable a complete link between the digital and real world.

IP (intellectual property): prefabricated, reusable circuit blocks or designs that can be integrated into larger chips. Examples are processor cores (e.g. ARM or RISC-V), interface modules (e.g. PCIe, USB) or memory controllers. IP can be licensed or internally developed.

Layout: the physical representation of a chip that contains the positions of the transistors, metal interconnects and other components. The layout is created in line with the fabrication technology's design rules and has to be optimised to improve space requirements and performance.

Leading-edge node: the latest and most advanced manufacturing technology for semiconductors, measured in nanometres (e.g. 5 nm, 3 nm). These nodes offer higher transistor density, better energy efficiency and higher performance, but are becoming increasingly complex due to rising costs and technical challenges.

LLM (large language model): a large neural network that has been trained for natural language processing. LLMs such as GPT or BERT can be used for documentation, design optimisation and automation in the semiconductor industry.

LVS: (Layout versus Schematic): As part of the design verification, it must be checked whether the layout created still corresponds to the circuit diagram (schematic) created in the previous step.

MCM (multichip module): a packaging approach in which a number of chips (dies) are integrated on a common carrier or substrate. MCMs enable higher performance and bandwidth by combining various functions in one module.

MEMS (microelectromechanical systems): microsystems that combine mechanical and electrical components on one chip. MEMS are used, for example, for sensors and micromirrors in projectors.

Mixed-signal: a field of design that combines both digital and analogue circuit elements. Mixed-signal ICs are often used in communications and sensor systems and in signal processing, for example in analogue-to-digital converters (ADC) or digital-to-analogue converters (DAC).

ML (machine learning): a field of artificial intelligence that uses algorithms to learn from data and to recognise patterns. ML is used in chip development for optimisation, verification and automated design.

Moore's law: an observation by Gordon Moore (co-founder of Intel) which states that the number of transistors on a chip doubles approximately every two years and was for many years reflected in exponential increases in performance and cost reductions in the semiconductor industry.

NDA (non-disclosure agreement): an agreement that ensures the confidentiality of information between two parties. An NDA is often required in the semiconductor industry in order to gain access to confidential documentation, design kits (PDKs) or technologies.

Netlist: a description of the electrical interconnects between the various components of a circuit that is used in electronic design automation to translate a chip's logical design into a physical implementation.

OS (open-source): a development model in which design files, software or hardware are made publicly available. In chip design, there are open-source EDA tools, open-source processor architectures (e.g. RISC-V) and open-source IP designs that foster transparency and collaboration.

Packaging: the process in which a finished semiconductor chip is embedded in a protective package (housing). Packaging provides mechanical stability, heat dissipation and electrical interconnects with the outside world. Modern technologies include 2.5D and 3D packaging that integrate a number of chips in one package.

Parasitic extraction: an analysis process for calculating unwanted electrical effects (parasitic resistances, capacitances or inductances) in the layout. These effects can have an impact on a chip's signal integrity and performance.

PDK (process design kit): a collection of data and rules provided by a semiconductor manufacturer to enable the design of chips for a specific manufacturing technology. A PDK contains, for example, design rules, simulation models and standard cell libraries.

Photonics: a field of semiconductor technology that deals with the integration of optical waveguides and optical components into chips. Photonics chips are used for high-speed data transmission, sensor technology and quantum computing.

Place and route: an important step in the chip design process in which the physical positions of the of the components on the silicon chip are determined (placement) and the electrical interconnects between them are produced (routing).

RF (radio-frequency): a field of chip design that deals with circuits for wireless communication, for example for mobile radio, WLAN or satellite communication. RF design requires special techniques to minimise noise and interference.

RRAM: (Resistive Random-Access Memory): This describes a type of non-volatile memory that stores information by changing the electrical resistance of a weakly conductive dielectric.

Schematic (circuit diagram): a graphical representation of an electronic circuit that shows how components are interconnected. Schematics are the foundation for circuit simulation and layout design.

Sign-off: the final step in the chip design process in which the design is checked before it is approved for fabrication. This includes timing analysis, DRC (design rule check), LVS (layout vs. schematic) and other verification steps.

SiP: (System-in-Package): This describes a group of integrated circuits (ICs) that have been combined together in a package.

SRAM (static random-access memory): fast, energy-efficient memory used in processor caches. In contrast with DRAM, SRAM does not require regular refreshing as data is stored in flip-flops.

Synthesis (logic synthesis): the process in which an abstract description of a digital design (e.g. in Verilog or VHDL) is automatically converted into a netlist of gates. Synthesis optimises the design in terms of area, speed and energy consumption.

TSMC (Taiwan Semiconductor Manufacturing Company): the world's leading semiconductor fabricator (foundry) that produces chips for many companies including Apple, NVIDIA and AMD. TSMC is pioneer in advanced fabrication processes such as 3 nm and 2 nm.

Validation: the process of ensuring that the developed product meets the end user's requirements. While verification checks whether the design has been implemented correctly, validation ensures that the correct design has been developed.

Verification: the process of checking whether a designed circuit or system functions correctly and meets specifications. This involves various methods such as simulation, formal verification and emulation.

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The design of modern electronic circuits is unthinkable without special design software. However, due to legal restrictions and high licensing costs, established proprietary solutions constitute a major hurdle for small companies and start-ups wishing to develop their own microchips. Open-source design tools offer an interesting alternative, although they do not yet meet industry's stringent requirements.

This publication examines the technologies and applications for which open-source design tools can be used in the future to enhance Europe's technological sovereignty and boost its innovation capacity.